CF+ and CompactFlash Specification Revision 4.1

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1 General

1.1 Introduction

The CompactFlash Association (CFA) was established in October 1995 with the premise that CompactFlash (CF) technology would enable the introduction of a new class of advanced, small lightweight, low power mobile products that would significantly increase the productivity and enhance the lifestyles of millions of people.

The concept behind CF technology was simple: to capture, retain and transport data, audio and images on CompactFlash Storage Cards. CF Storage Cards provided the capability to easily transfer all types of digital information and software between a large variety of digital systems. The CFA approved and published the CompactFlash standard. This vendor-independent specification enabled users to develop CF products that function correctly and are compatible with future CF designs, eliminating compatibility issues.

Now the CFA has developed the CF+ specification to expand the CF concept beyond flash data storage and include I/O devices and magnetic disk data storage. The CF+ specification also includes the original Type I (3.3 mm thick) card and newer Type II (5 mm thick) cards. While CompactFlash and many I/O devices can fit into the Type I card, the Type II cards enable higher capacity CompactFlash cards, magnetic disk cards and many additional I/O cards.

1.2 CFA Goals and Objectives

The goals of the CFA are to promote and encourage the worldwide adoption of CF+ and CompactFlash (CF) technology as an open standard. The association's primary objectives are to drive second-source availability; to promote acceptance of the CF+ specification as an industry standard across platforms and markets internationally; to ensure compatibility for users of CF and CF+ products, and to evolve the approved CF+ standard over time while ensuring backward compatibility.

1.3 Overview of CompactFlash Storage Card

CF+ is a small form factor card standard that encompasses CompactFlash (CF) flash data storage cards, magnetic disk cards and I/O cards including, but not limited to serial cards, Ethernet cards, fax/modem cards and wireless pager cards.

The CF+ card provides high capacity data storage and I/O functions that electrically comply with the Personal Computer Memory Card International Association standard. (In Japan, the applicable standards group is JEITA.) Minor differences between the CF+ Specification and the PC Card ATA standard are documented in the Appendix at the end of this specification. Although the size of a matchbook, CF+ and CompactFlash Cards can be used with passive adapters in a PC-Card Type II or Type III socket.

A CompactFlash Storage Card also runs in True IDE Mode that is electrically compatible with an IDE disk drive. Other CF+ devices such as magnetic disk drives may also run in True IDE Mode.

The CompactFlash Storage Cards on-card intelligent controller manages interface protocols, data storage and retrieval as well as Error Correcting Code (ECC), defect handling and diagnostics, power management and clock control. Once the CompactFlash Storage Card has been configured by the host, it appears to the host as a standard ATA (IDE) disk drive.

Similar controller functions are used with other CF+ cards allowing a wide variety of devices to be compatible with the CF+ specification

1.4 Related Documentation

- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification, 1995
- PCMCIA Metaformat Specification, 1997
- PCMCIA Physical Specification Revision 7.0, 1999

  These documents can be obtained from:

  PCMCIA
  2635 North First St., Ste. 209
  San Jose, CA 95131 USA
  Phone: 408-433-2273
  Fax: 408-433-9558

- AT Attachment Interface Document, American National Standards Institute, X3.221-1994
- ANSI NCITS 317-1998 AT Attachment - 4 with Packet Interface
- ANSI INCITS 361-2002 AT Attachment - 6 Annex C Signal Integrity and UDMA Implementation Guide

  Copies of the ATA standards can be purchased from:

  ANSI
  11 West 42nd Street
  New York, NY 10036 USA
  Tel: 212 642-4900

  or

  Global Engineering Documents
  Inverness Way East
  Englewood, CO 80112-5704
  Tel: 800 854-7179
  Outside USA and Canada 303 792-2181
  International Sales Fax: 303 397-2740.

  Additional references can be found in the Bibliography at the end of this specification.

1.5 Compatibility Requirements

CompactFlash and CF+ are trademarks of the CompactFlash Association. All products that conform to this specification may use the CompactFlash and CF+ names with the appropriate license from the CompactFlash Association.

The goal of this specification is to conform to the PC Card Specification when operating in the PCMCIA PC Card modes and to conform to the ATA-4 specification when operating in the True IDE Mode. If there is a conflict between this specification and the PC Card or the ATA-4 Specifications, the CompactFlash Specification shall apply.

To conform to this specification, a CompactFlash Storage Card or CF+ Card shall conform to all physical, electrical and Metaformat specifications in this document. A CompactFlash Storage Card shall implement all PC Card and True IDE ATA commands listed in this specification. Commands can be implemented as “no operation” to meet this requirement.

1.6 Acknowledgement

The CompactFlash Association is pleased to acknowledge the technical contributions made to the CompactFlash specification by member companies and the following individuals:

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Yasuro Kubota
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Hongning Yang

2 Scope

2.1 Elements of this Specification

This specification is divided into five sections: Card Physical, Electrical Interface, Metaformat, Software Interface and CompactFlash Adapter. A brief overview of each section follows.

2.2 Card Physical

This section defines the dimensions and mechanical tolerances for CompactFlash Storage Cards and CF+ Cards. Specific pin lengths are defined to ensure that power is applied first and removed last during card insertion and removal. Reliability factors, such as connector mate/unmate cycles, environmental operating conditions and test methods are also specified.

2.3 Electrical Interface

This section provides detailed pinout and signal definitions for Memory Mode, I/O Mode and True IDE Mode CF Storage and CF+ Cards. Detailed functional and timing information is provided including the provision for reading 16 bit data on the low order 8 data bits (useful in 8 bit host systems) and the interpretation of status information returned by the CF Storage Card or CF+ Card.

2.4 Metaformat

This section describes the Card Information Structure (CIS), or Metaformat, on CompactFlash Storage Cards and CF+ Cards and how to interpret the Metaformat for the purpose of configuring and utilizing the card.

2.5 Software Interface

This section describes the software interface between the host and the CompactFlash Storage Card. This section does not apply to all CF+ Cards.

2.6 CompactFlash Adapters

This section describes the passive Type II PCMCIA adapters that can be used with the Type I or Type II CompactFlash Storage Card or CF+ Card.

3 Card Physical

3.1 General Description

3.1.1 CompactFlash Storage Card

The CompactFlash Storage Card contains a single chip controller and flash memory module(s) in a matchbook-sized package with a 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27 mm) centers. The controller interfaces with a host system allowing data to be written to and read from the flash memory module(s).

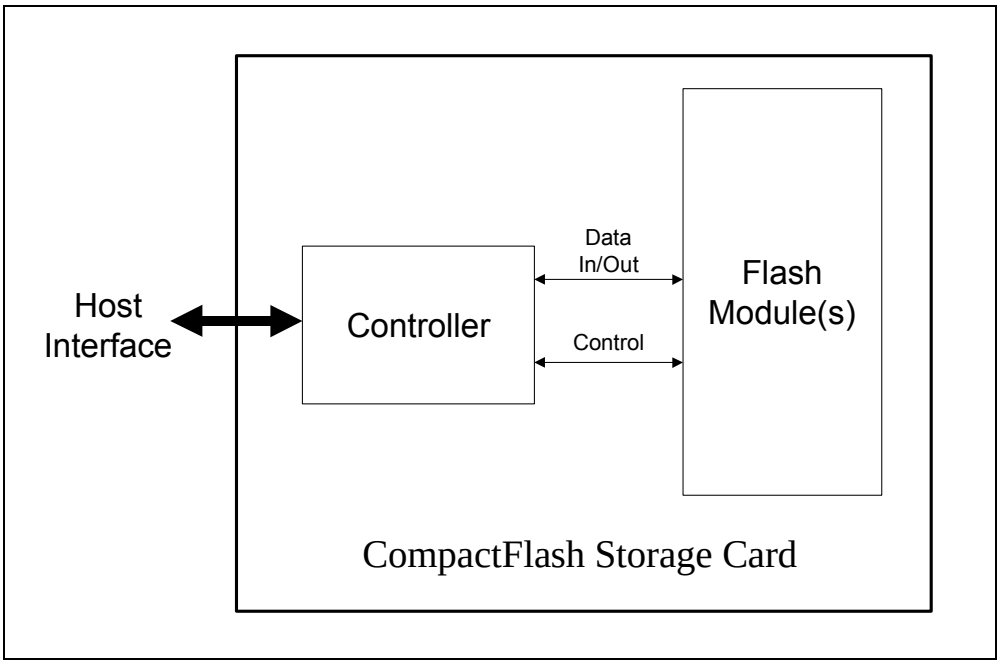


Figure 1: CompactFlash Storage Card Block Diagram

3.1.2 CF+ Card

The CF+ card contains functions other than ATA flash memory, such as I/O (serial port, modem, LAN, etc) or non-flash storage (hard disk drive). Physical specifications are identical to CompactFlash cards (either Type I or Type II).

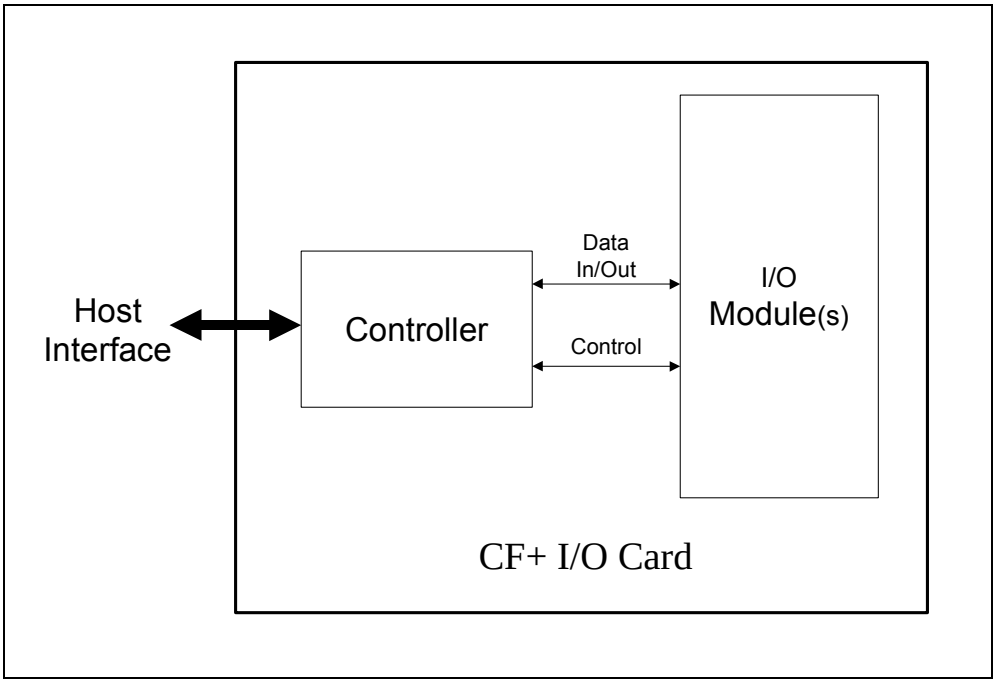


Figure 2: CF+ Card Block Diagram

3.2 CompactFlash Storage Card and CF+ Card Physical Specifications

3.2.1 CF+ & CompactFlash Type I and Type II Cards

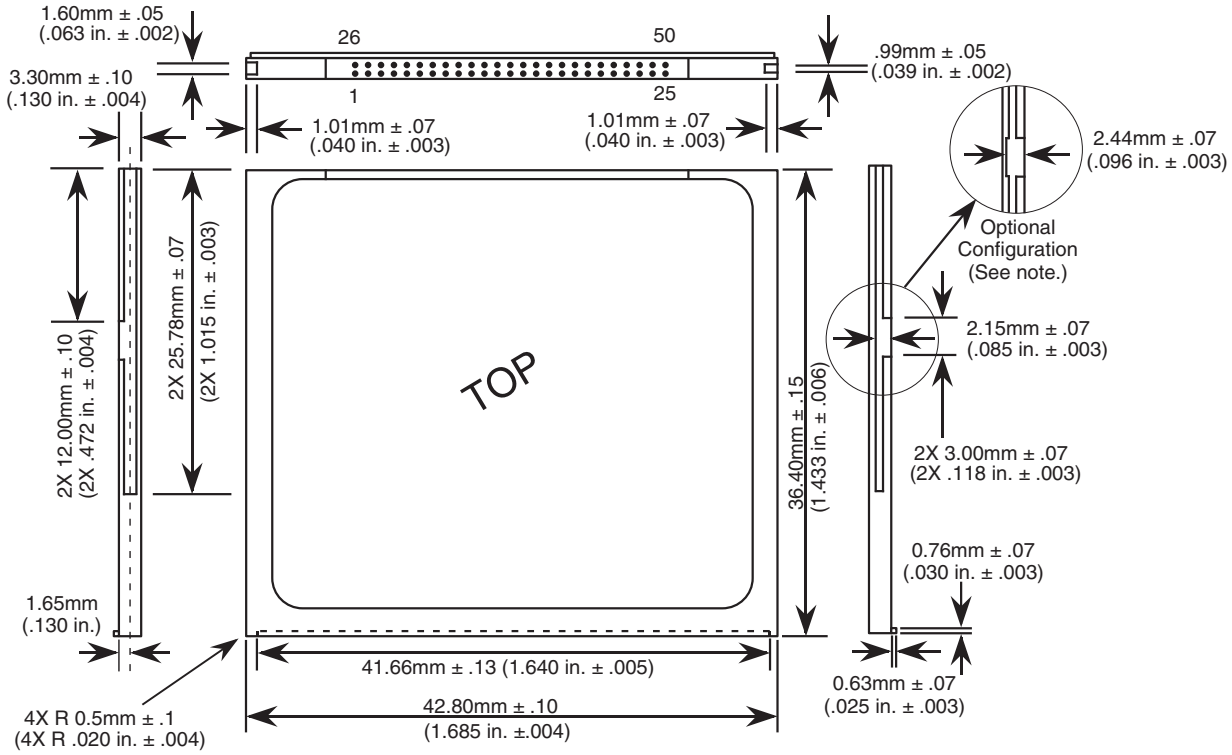
Refer to Table 1, Table 2: Type II CompactFlash Storage Card and CF+ Card Physical Specifications, Figure 3 and Figure 4 for the CompactFlash Storage Card and the CF+ Card dimensions and physical specifications.

Table 1: Type I CompactFlash Storage Card and CF+ Card Physical Specifications

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness Including Label Area:	3.3 mm ± 0.10 mm (.130 ± .004 in.)

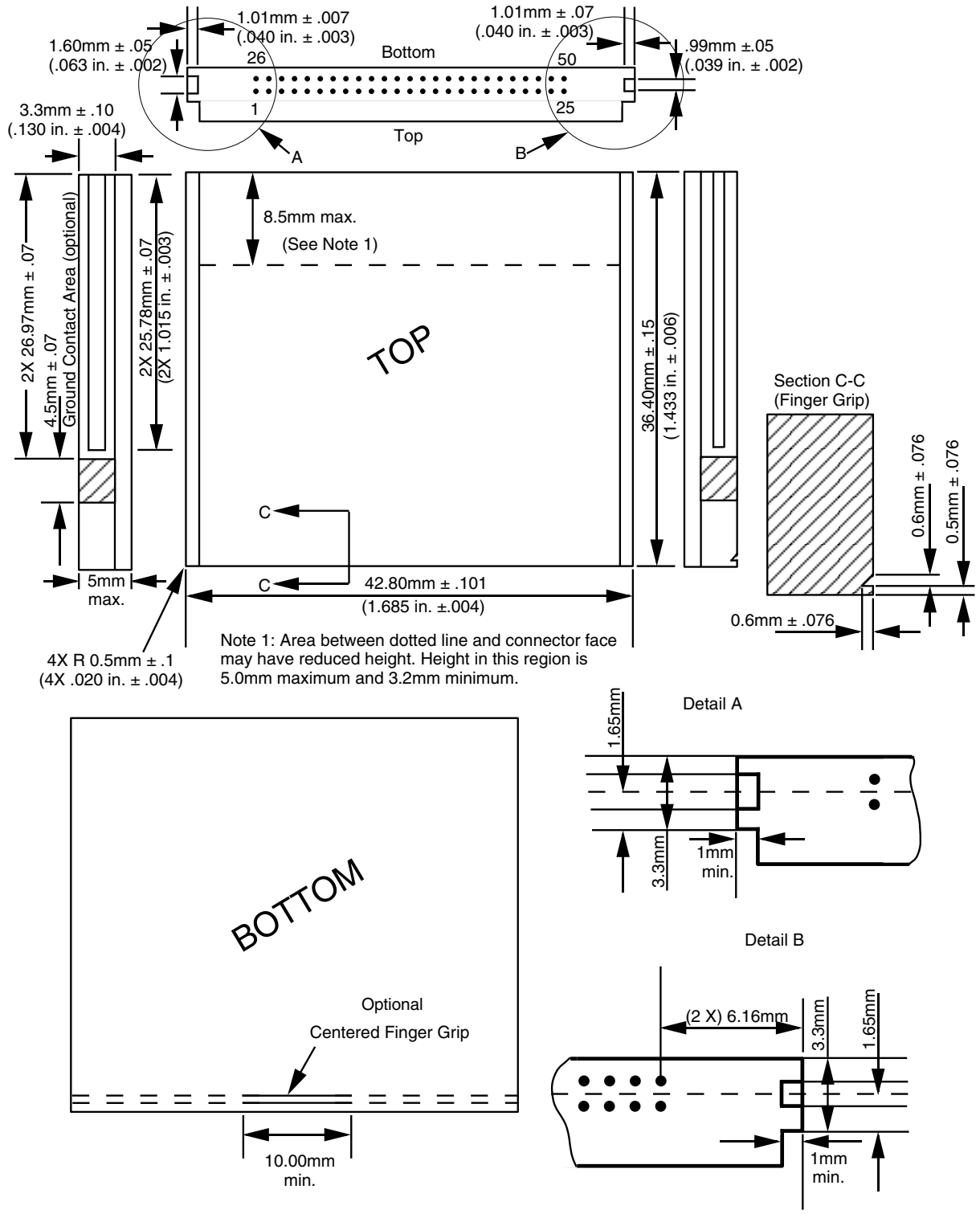
Table 2: Type II CompactFlash Storage Card and CF+ Card Physical Specifications

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness Including Label Area:	5.0 mm maximum (.1968 in. maximum)



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

Figure 3: Type I CompactFlash Storage Card and CF+ Card Dimensions



Note: the recessed centered finger grip (Section C-C) is optional although it is recommended for CF+ Type II cards. Additionally, it is recommended that Type II host slots include an ejector mechanism.

Figure 4: Type II CompactFlash Storage Card and CF+ Card Dimensions

3.2.2 Recommendations for Longer Type I and Type II Cards

Both Type I and Type II CompactFlash Storage Cards and CF+ Cards may be lengthened beyond the 36.4 mm dimension. It is often desirable to include a bump up above the 3.3 mm or 5 mm thickness as well. If the thickness is to be increased, it shall not be increased until after 39.5 mm from the 50-pin connector and then increase at a 120º angle. Refer to Figure 5 and Figure 6 for dimensions.

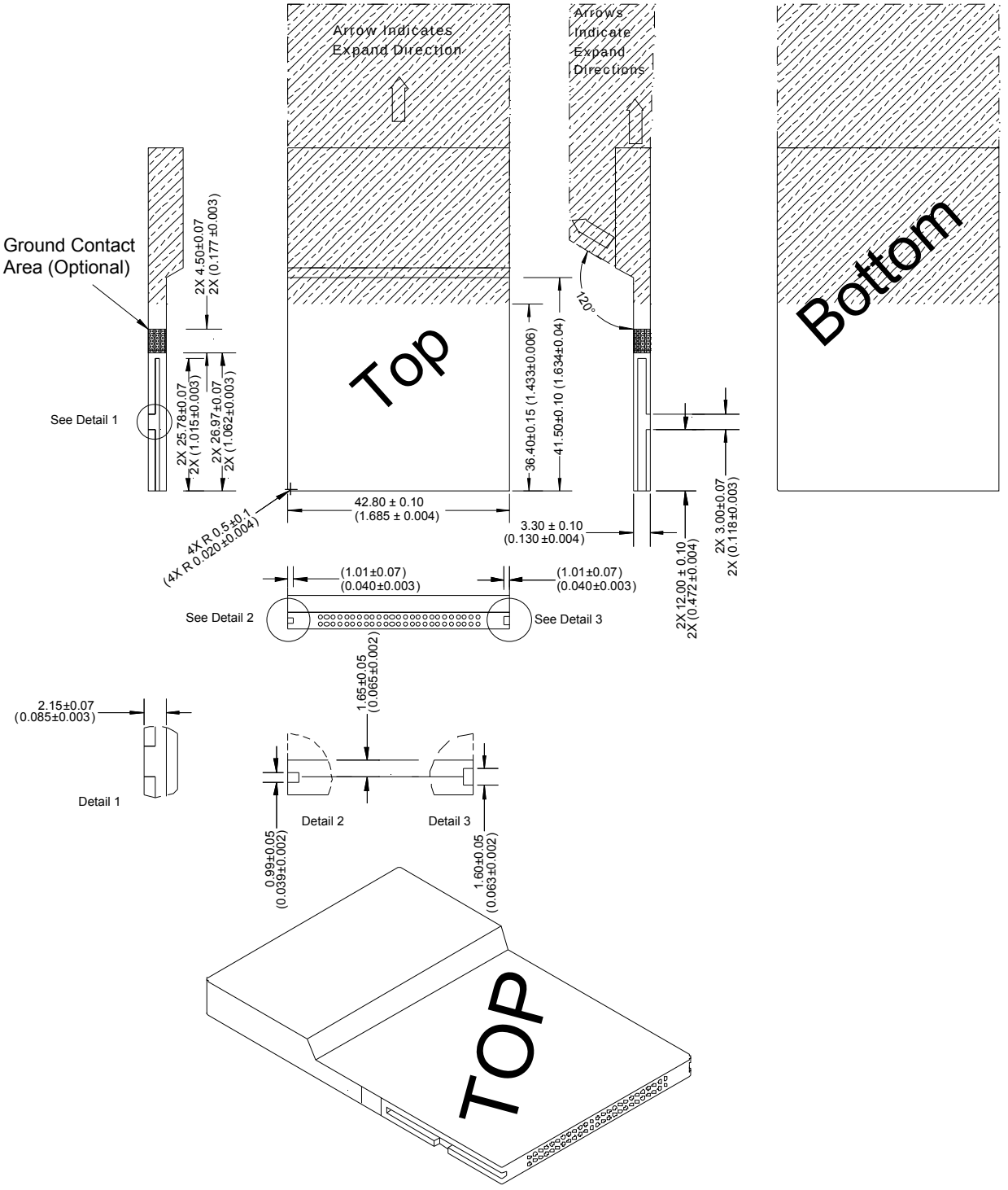


Figure 5: Longer Type I CompactFlash Storage Card and CF+ Card Dimensions

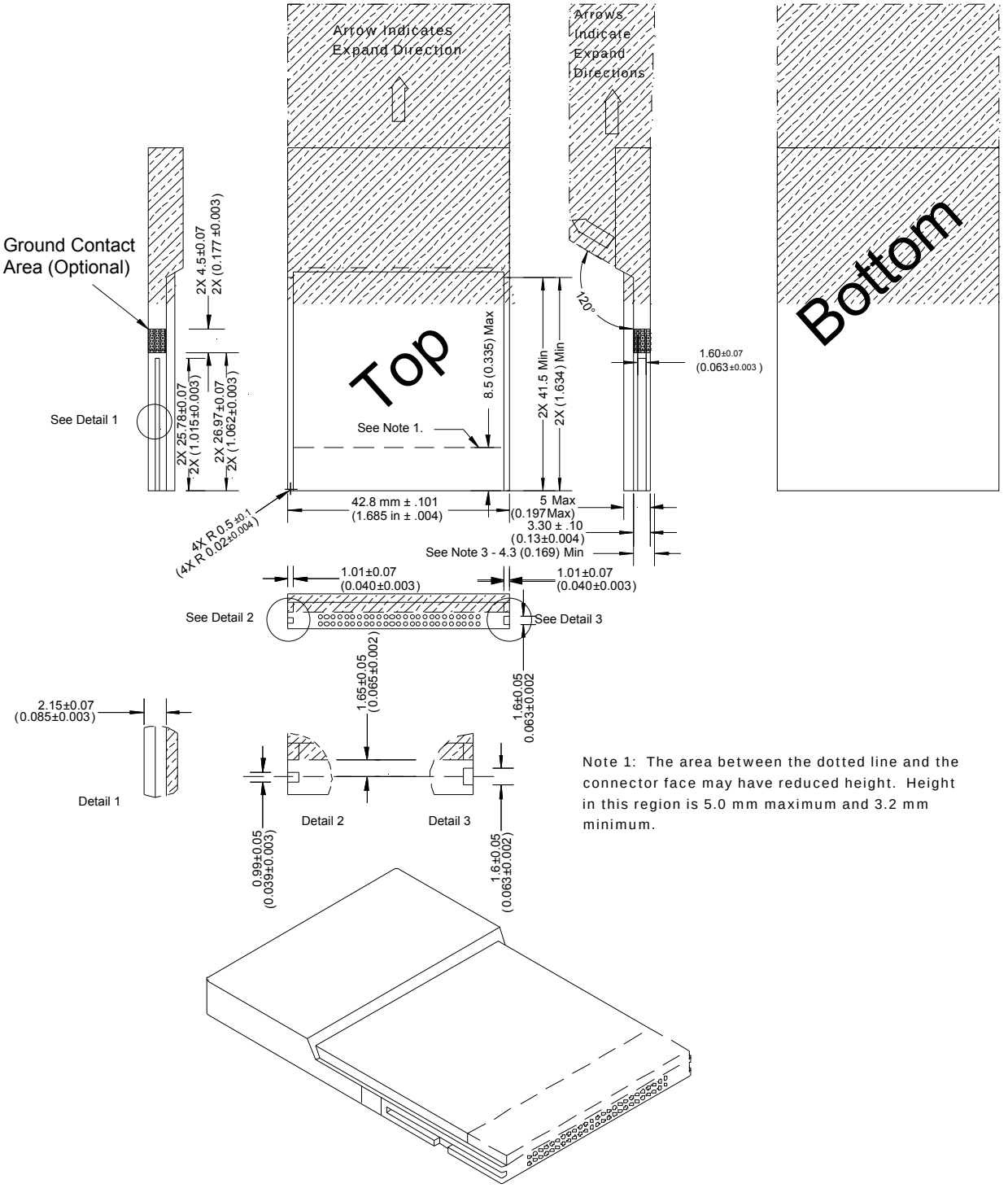


Figure 6: Longer Type II CompactFlash Storage Card and CF+ Card Dimensions

3.2.3 CF+ Type I Extended

Type I Extended is an optional physical format that allows for a thicker card along almost the entire length of a CF Type I card. A CF+ Type I Extended card has the same width and rails as a

Type I card; however, it can be extended in thickness (on the bottom) and in length. Refer to Figure 7 for allowable dimensions and recommendations.

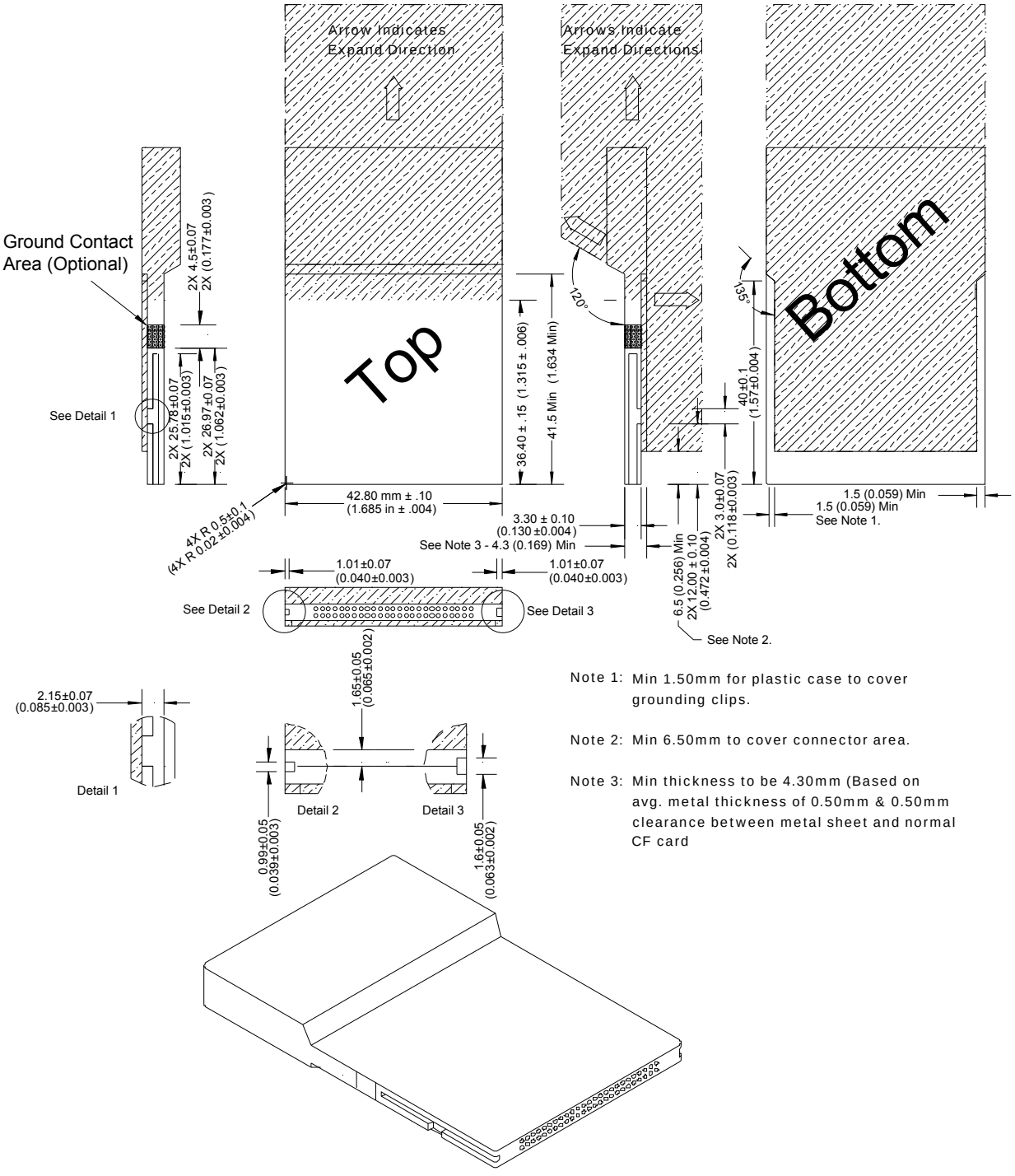


Figure 7: CF+ Extended Card Dimensions

3.3 Connector Interface Specifications

The specified CF Card connector interface shall be a 50-position, 2-piece pin-and-socket. The socket contacts shall be within the CF Card connector. The outermost plating of the pin and socket contact areas shall be a noble metal that is compatible with gold, and shall meet the performance requirements specified in Table 3: Connector Interface Requirement.

Within this specification, the geometric plane established by the face of a fully engaged socket on its host connector is defined as "Datum A." To evaluate interchangeability among various connectors, dimensional layouts should be referenced from Datum A, i.e., the CF Card Socket face or the CF Card Slot Header floor.

Table 3: Connector Interface Requirement

Category	Item	Standard	Test Method
Physical	Housing Material	High Temperature Plastic	
	Housing Flammability Rating	UL 94V-0	Certification
Electrical Performance	Contact Resistance (w/ bulk)	40 milliohms maximum, initial 20 milliohms maximum change, throughout testing	EIA-364-23A
	Current Rating	0.5 Amperes per contact, without exceeding 30°C temperature rise above ambient	IEC-512-PT3
	Insulation Resistance	1000 Megohms minimum, initial 100 Megohms minimum, after 1 minute @ 500 Vdc	EIA-364-21A
	Dielectric Withstanding Voltage	No shorting during 1 minute @ 500 Vac rms, with 1 mA maximum current leakage	EIA-364-20A
Mechanical Performance	Single Socket Holding Force	4.9 N minimum push out @ 25 mm/minute	EIA-364-29A
	Single Pin Holding Force	9.8 N minimum push out @ 25 mm/minute	EIA-364-29A
	Total Mating Force	28.8 N maximum at 25 mm/minute	EIA-364-13A
	Total Inverse Mating Force	43.2 N minimum	PCMCIA-Rev 7.0-Card Physical Section 9.3.11
	Total Unmating Force	4.9 N minimum and 24.5 N maximum at 25 mm/minute	EIA-364-13A
	Durability	10,000 mating cycles, without exceeding low-level contact resistance	EIA-364-09B
Environmental Performance	Mechanical Shock	No discontinuities greater than 100 ns, Test Condition A	EIA-364-27A
	Vibration	No discontinuities greater than 100 ns, Test Condition III	EIA-364-28A
	Humidity	10 (24 hour) cycles with connector mated	EIA-364-31A
	Thermal Shock	-55°C to +85°C, 5 (1 hour) cycles	EIA-364-32B
	Mixed Flowing Gas	Environmental Class II for 96 hours with connector unmated	EIA-364-65

3.3.1 CF/CF+ Card Connector

The socket-connector shall be located in the CF/CF+ Card as shown in Figure 3 and Figure 4. The CF/CF+ Card socket-connector interface layout shall match the host pin-connector layout as shown in Figure 8. The pin entry ports on the CF/CF+ Card socket-connector shall be configured as shown in Figure 9. The location of "first wipe on pin engagement" within the CF/CF+ Card socket-connector is shown in Figure 10.

The mechanical outlines for CF/CF+ Card Sockets are Figure 11: Straddle Mount CF/CF+ Card Socket and Figure 12: Surface Mount CF/CF+ Card Socket.

3.3.2 Host Connector

The host (CF/*CF*+ Card slot) pin-connector shall be a 50-pin connector with opening, polarization, and pin location as shown in Figure 13. The pin size and shape shall be as shown in Figure 14. The type and length for each pin number is shown in Figure 10.

If the host is a Type II PCMCIA PC Card, the pin-connector shall also conform to the physical specifications in Section 7.2 CompactFlash Adapter Specifications.

In all cases, the CF/*CF*+ Card shall be guided by the host connector for a minimum of 6.5 mm before the socket connector fully seats on the host connector. To ensure alignment of the CF/*CF*+ Card to the host connector, the CF/*CF*+ Card shall be guided for a minimum distance of 19.0 mm before engagement.

The mechanical outlines for CF/*CF*+ Card slot connectors are Figure 15: Straddle Mount CF/CF+ Card Adapter Header, Figure 16: Surface Mount Right Angle CF/CF+ Type I Card Slot Header and Figure 17: Surface Mount Right Angle CF/CF+ Type II Card Slot Header. Recommended Pad or Hole PCB Patterns for various tail configurations and mounting methods are shown in Figure 18 to Figure 22.

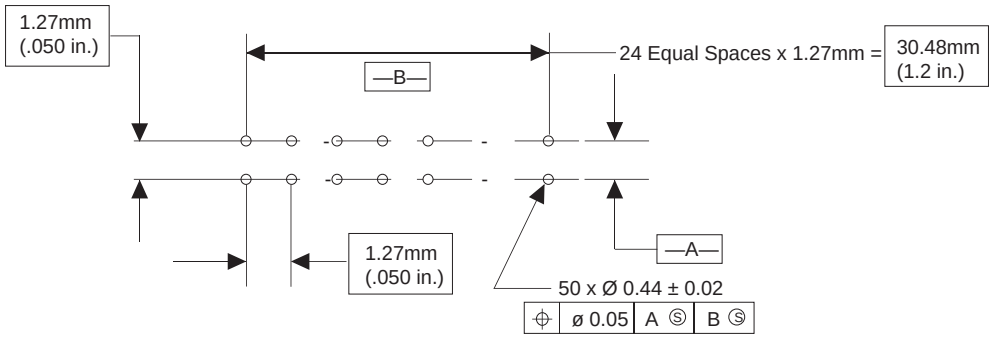


Figure 8: Position 2 Row Pin Pattern

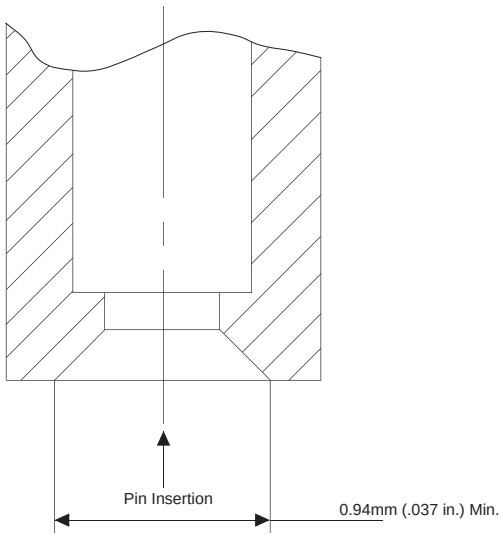
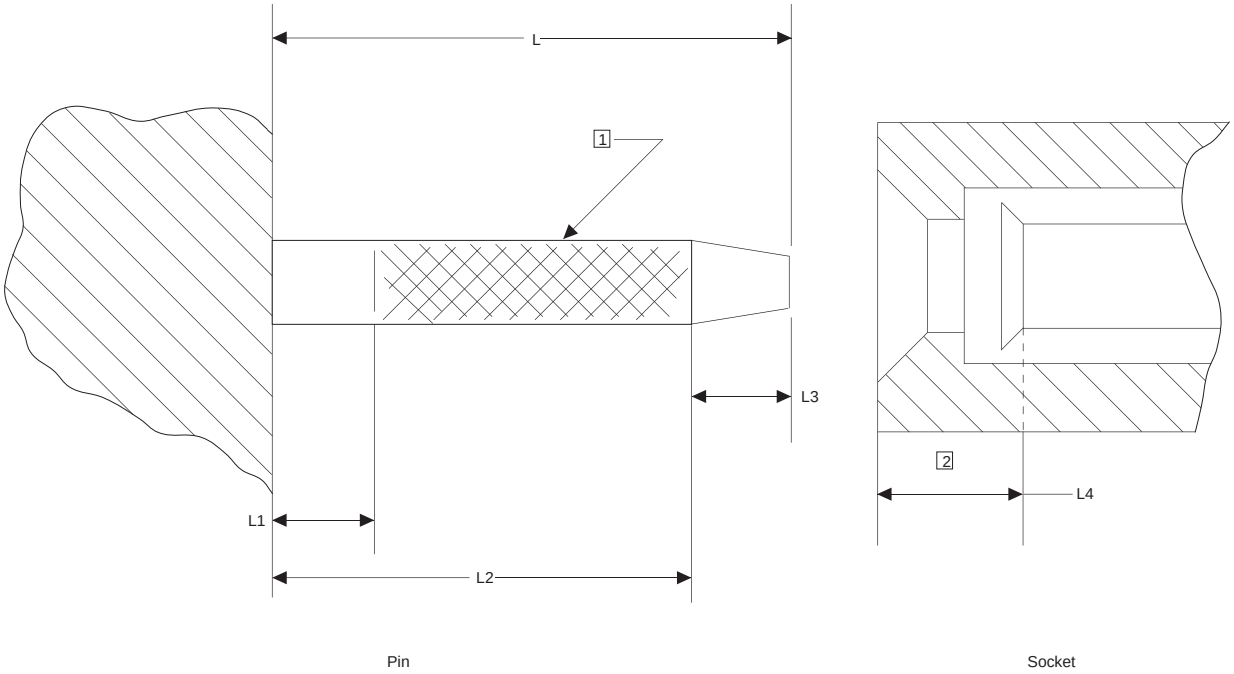


Figure 9: Socket Connector Entry

Description	Pin Number	L ± 0.10	L1 Max	L2 Ref	L3 ± 0.10	L4
Power	1, 13, 38 & 50	5.00 [.197]	0.50 [.020]	4.50 [.177]	0.50 [.020]	0.50 - 2.50 [.020 - .098]
General	All other pins	4.25 [.167]	0.50 [.020]	3.75 [.148]	0.50 [.020]	0.50 - 2.50 [.020 - .098]
Detect	25, 26	3.50 [.138]	0.50 [.020]	3.00 [.118]	0.50 [.020]	0.50 - 2.50 [.020 - .098]



Notes:
1 Pin/Socket contact area.
2 L4 is the point of first engagement for mating with the socket contacts/housing mounted within the card.

Figure 10: Pin and Socket Detail

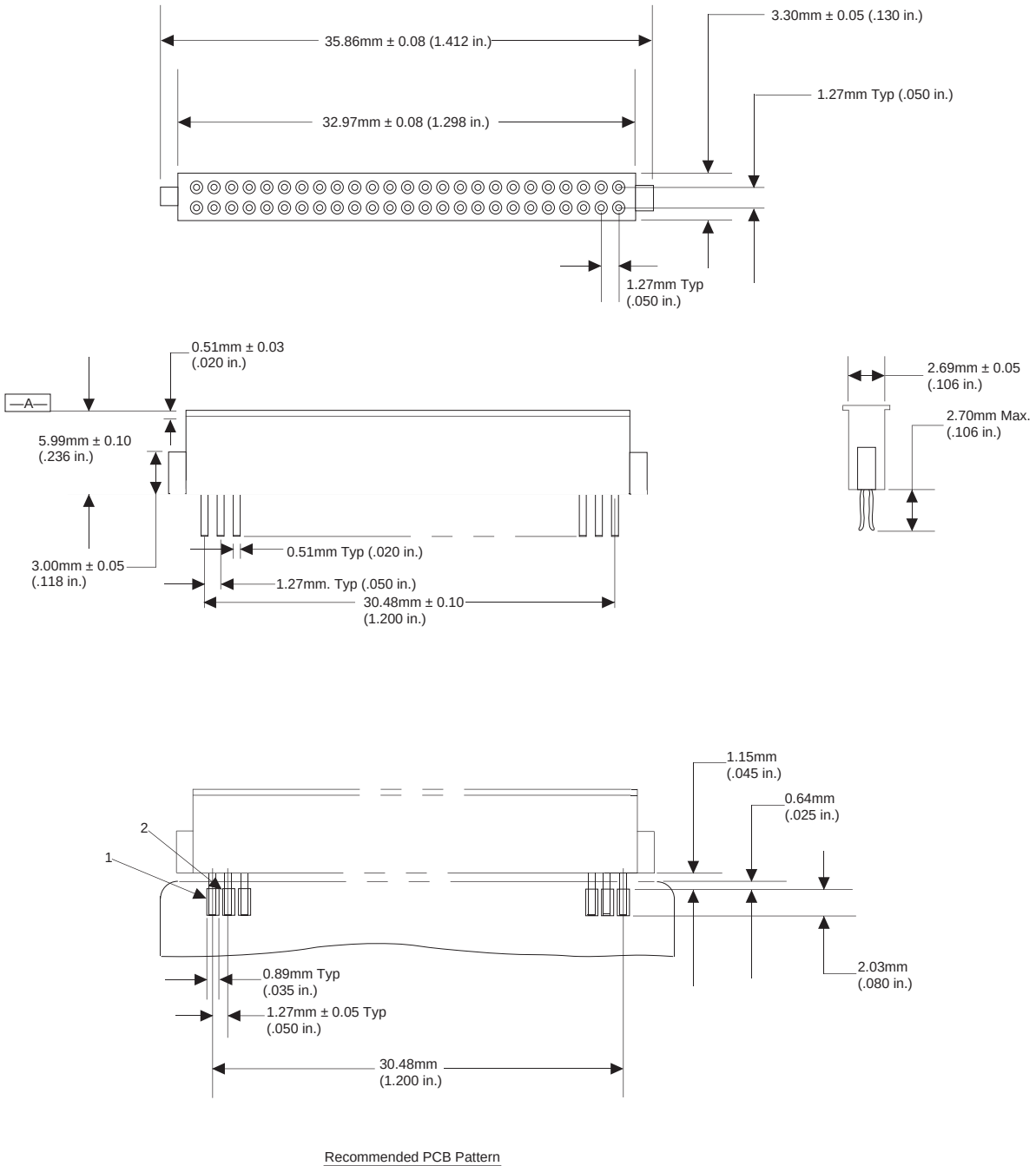


Figure 11: Straddle Mount CF/CF+ Card Socket

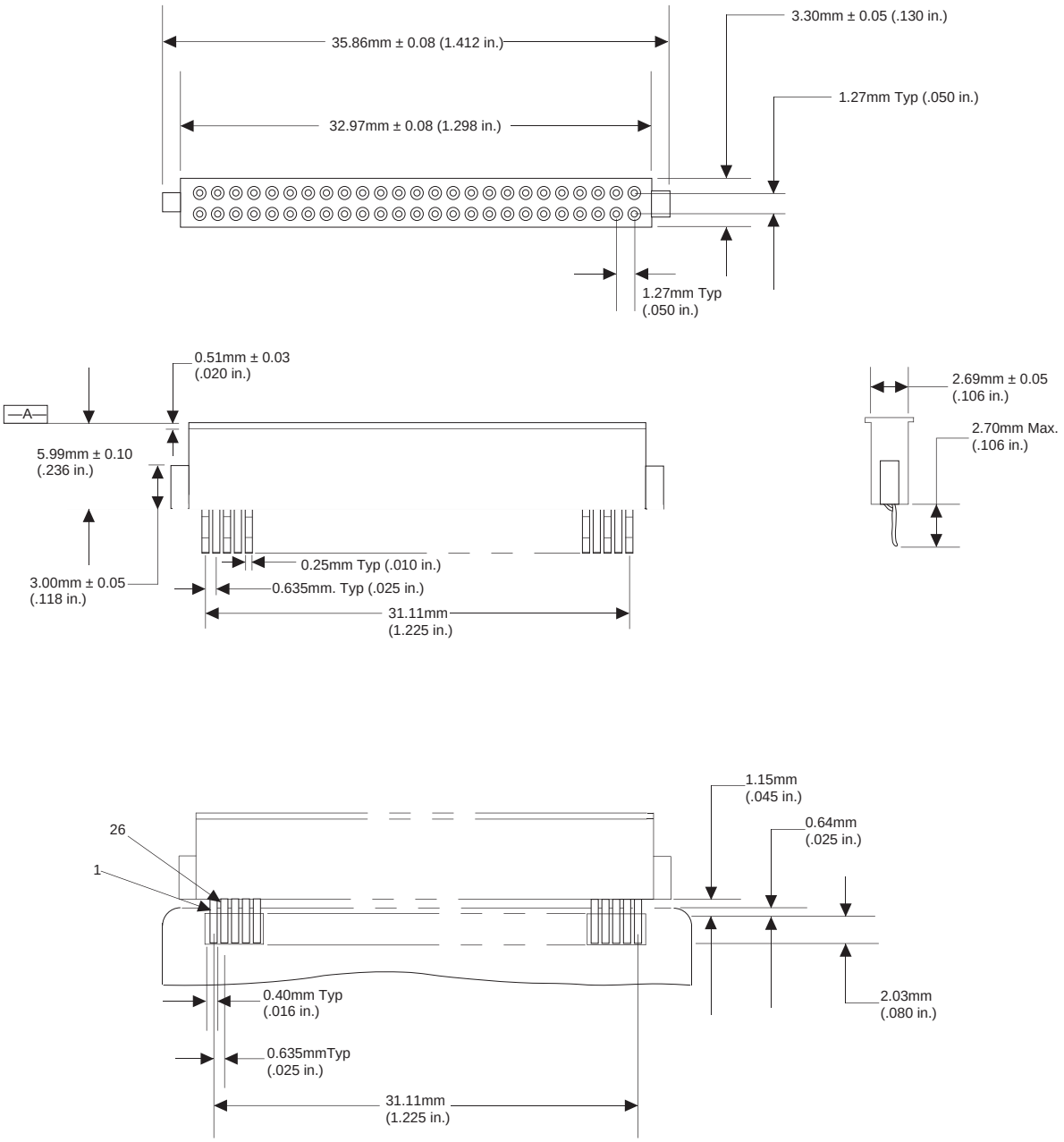


Figure 12: Surface Mount CF/CF+ Card Socket

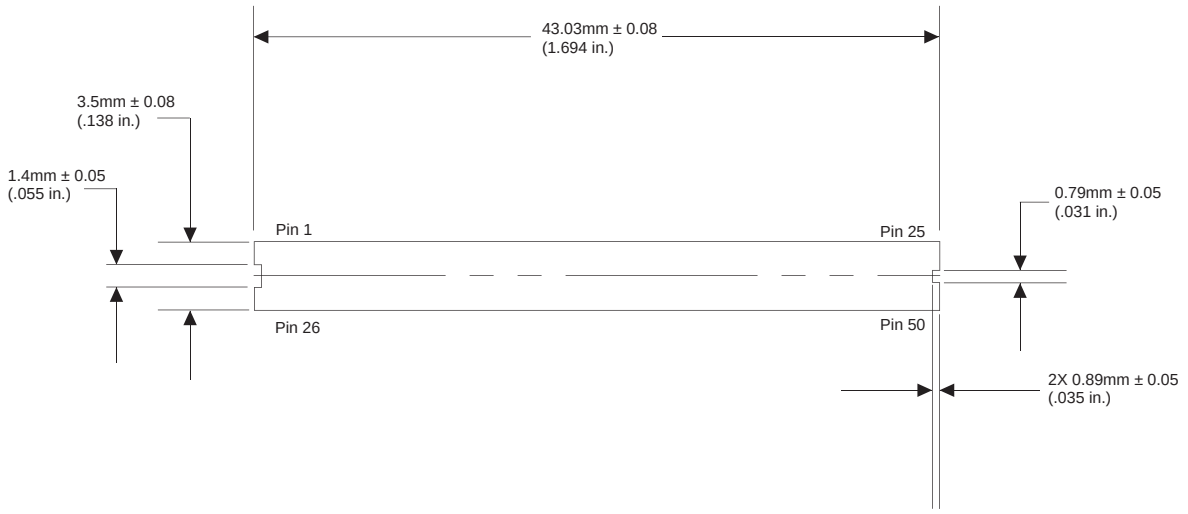


Figure 13: 50-Pin Connector Opening

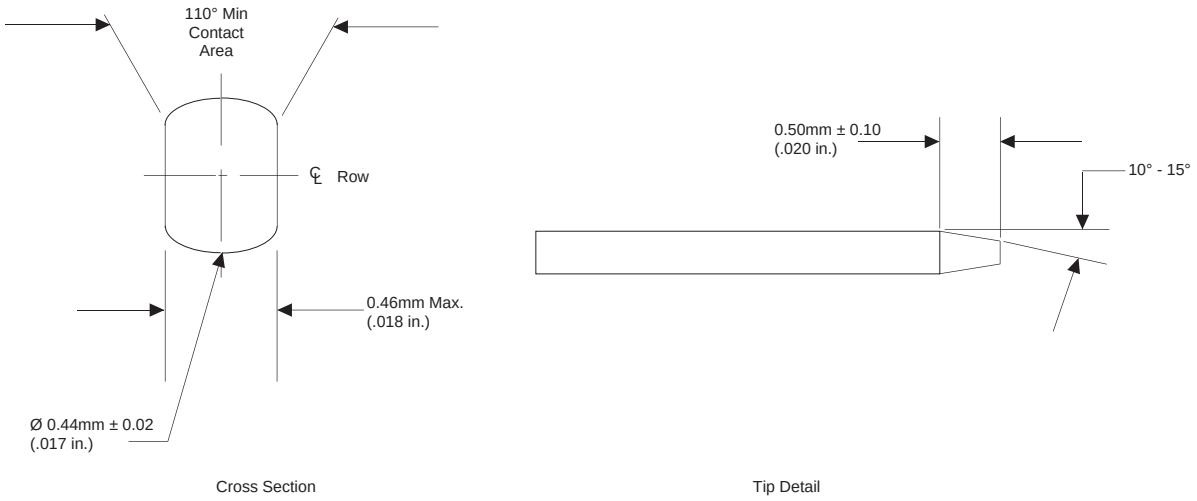


Figure 14: Header Pin Detail

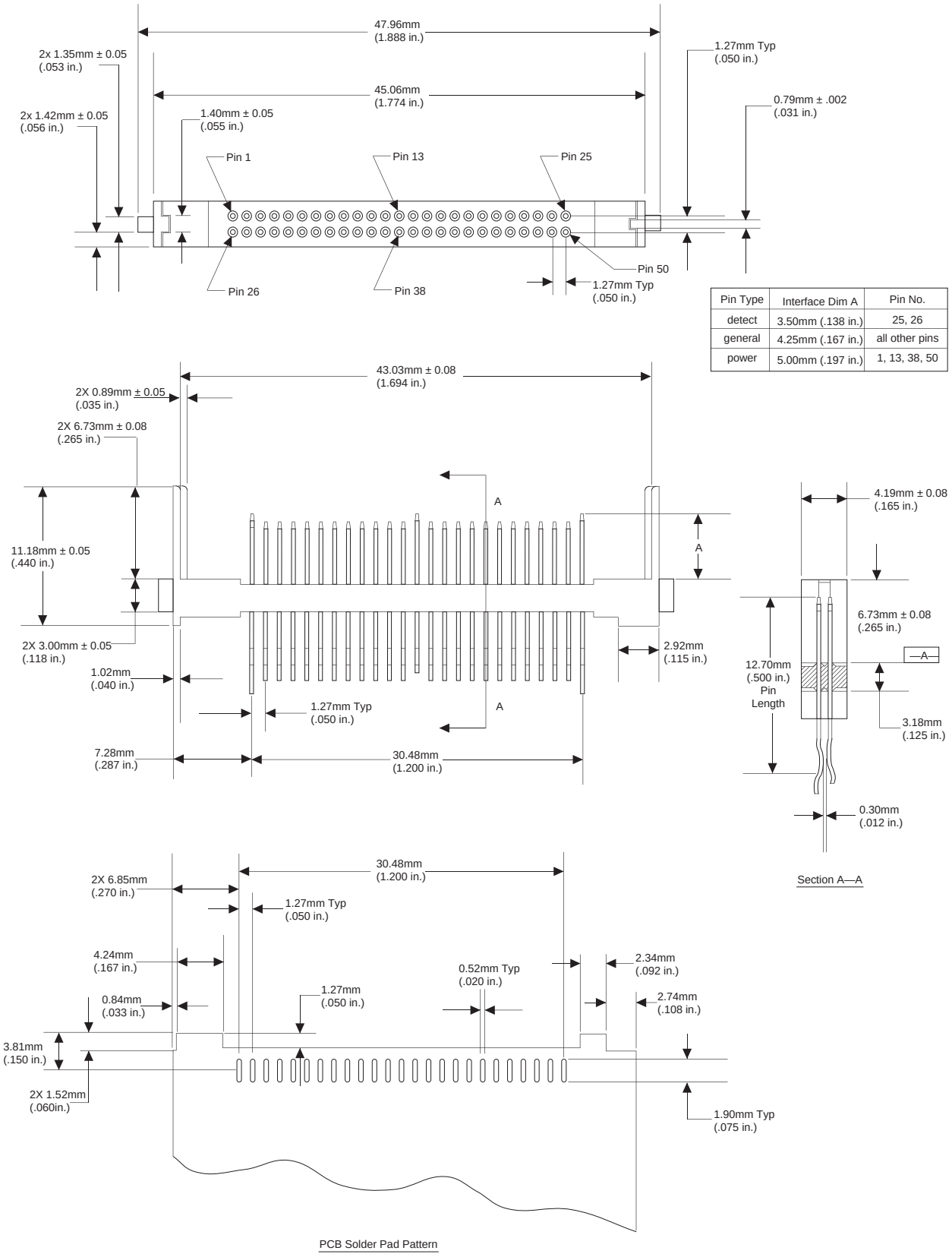


Figure 15: Straddle Mount CF/CF+ Card Adapter Header

Pin Type	Interface Dim A	Pin No.
detect	3.50mm (.138 in.)	25, 26
general	4.25mm (.167 in.)	all other pins
power	5.00mm (.197 in.)	1, 13, 38, 50

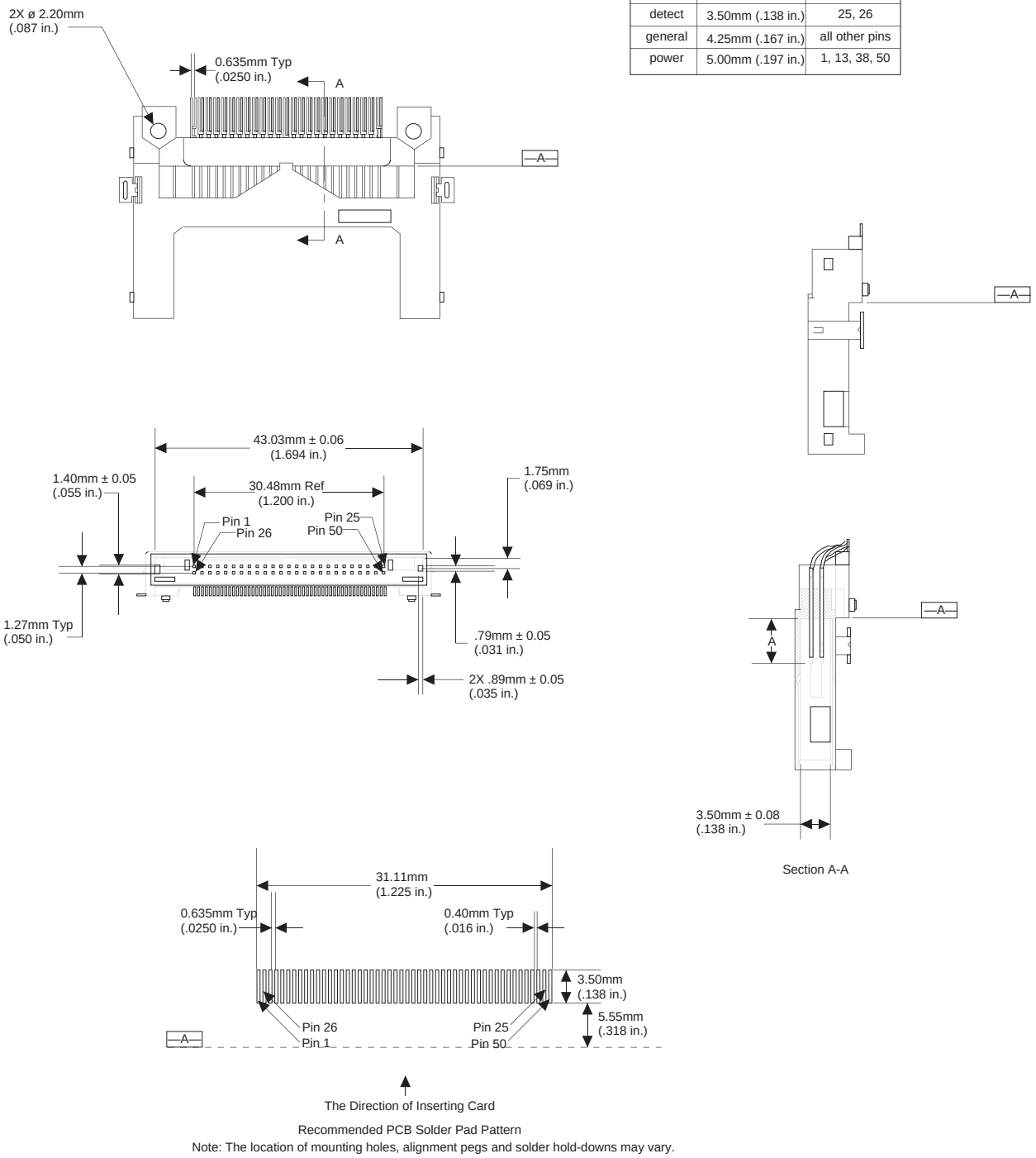
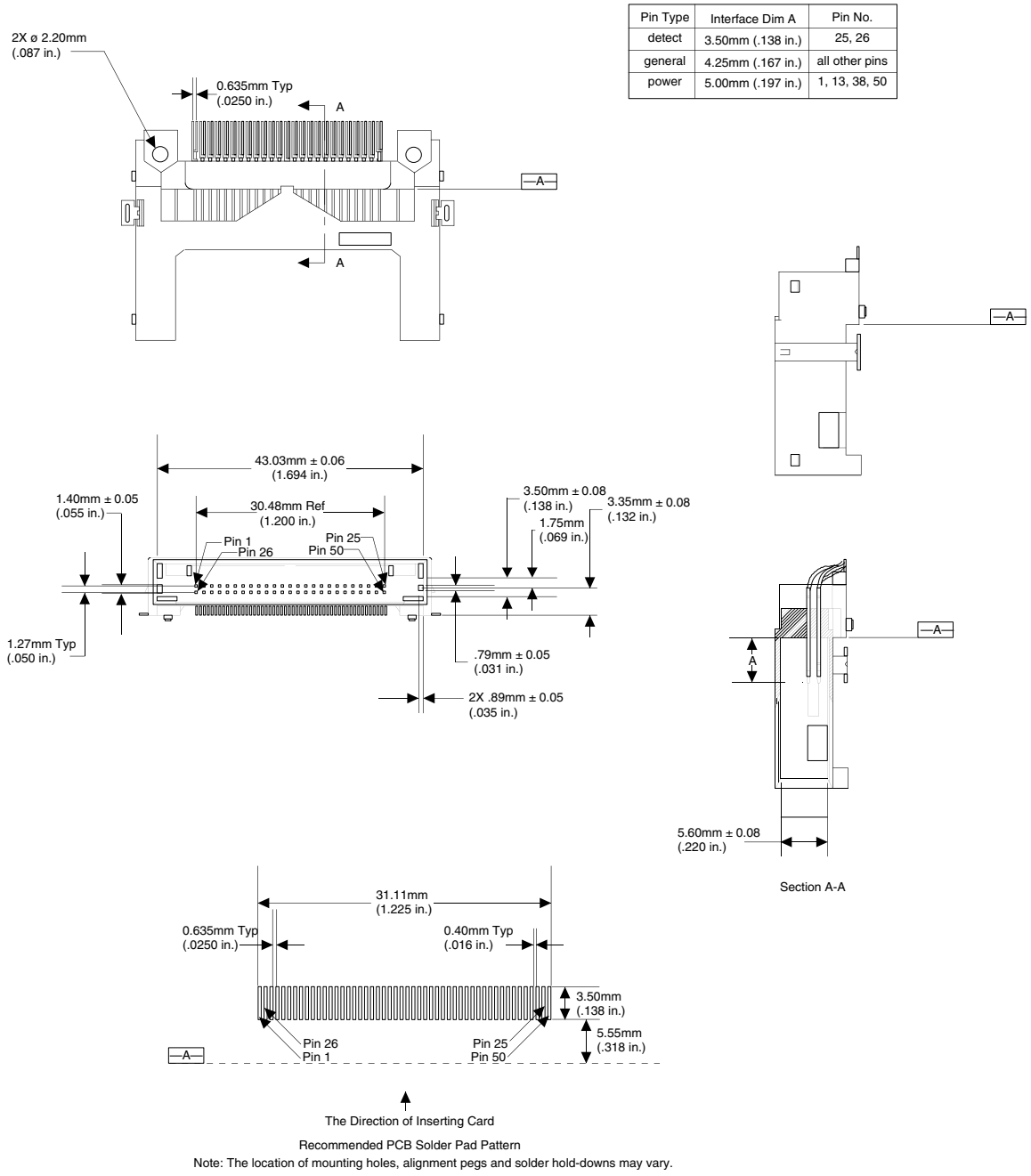


Figure 16: Surface Mount Right Angle CF/CF+ Type I Card Slot Header



Pin Type	Interface Dim A	Pin No.
detect	3.50mm (.138 in.)	25, 26
general	4.25mm (.167 in.)	all other pins
power	5.00mm (.197 in.)	1, 13, 38, 50

Recommended PCB Solder Pad Pattern

Note: The location of mounting holes, alignment pegs and solder hold-downs may vary.

Figure 17: Surface Mount Right Angle CF/CF+ Type II Card Slot Header

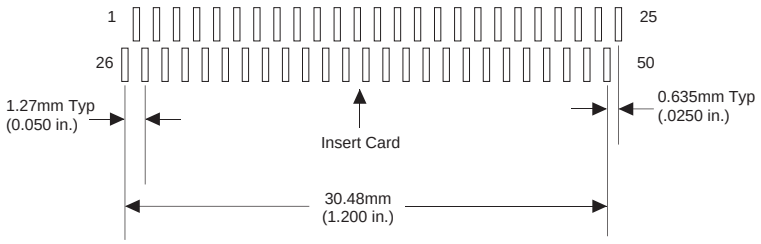


Figure 18: Two Row SMT Host PCB Pattern

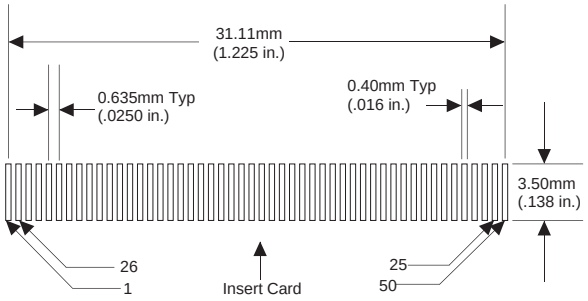


Figure 19: Single Row SMT Host PCB Pattern

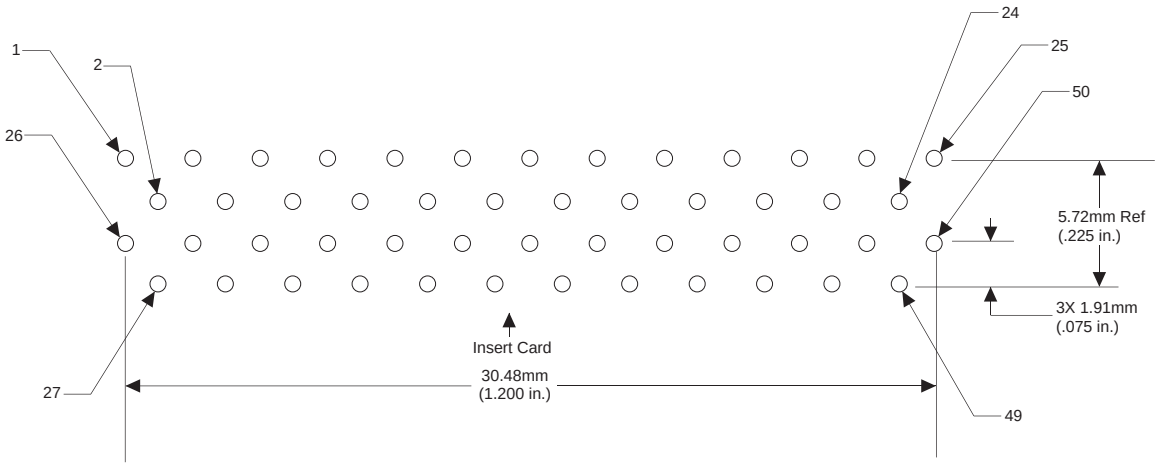


Figure 20: Right Angle Through Hole Host PCB Pattern

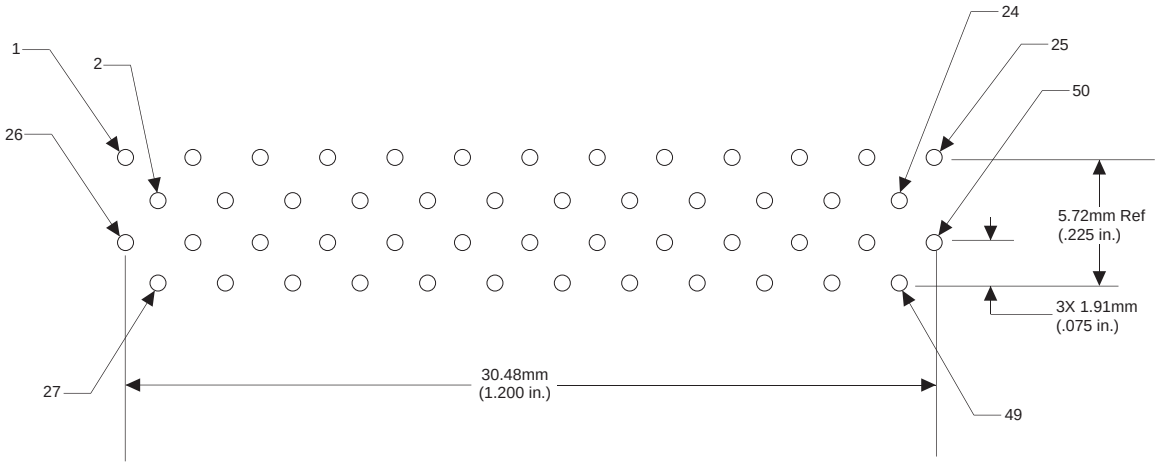


Figure 21: Vertical Through Hole Host PCB Pattern

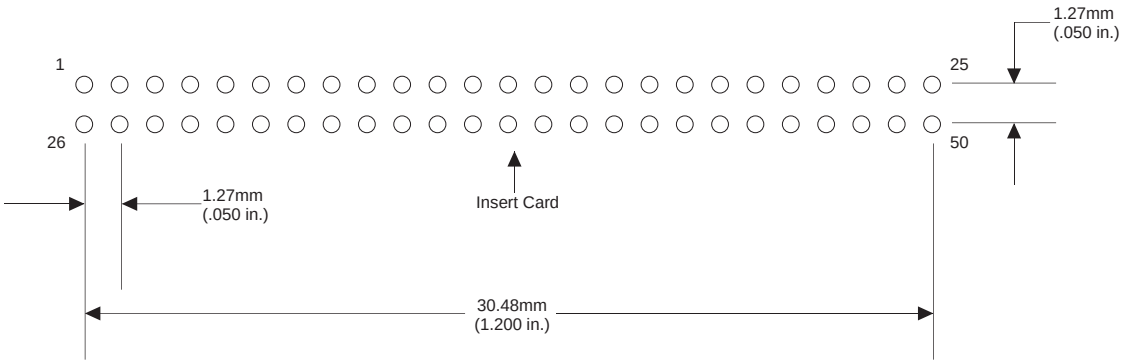


Figure 22: Alternate Right Angle Through Hole Host PCB Pattern

4 Electrical Interface

4.1 Physical Description

The host is connected to the CompactFlash Storage Card or CF+ Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

4.1.1 Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 4. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. *Section* 4.3 defines the DC characteristics for all input and output type structures.

4.2 Electrical Description

The CompactFlash Storage Card functions in three basic modes: 1) PC Card ATA using I/O Mode, 2) PC Card ATA using Memory Mode and 3) True IDE Mode, which is compatible with most disk drives. CompactFlash Storage Cards are required to support all three modes. The CF+ Cards normally function in the first and second modes, however they can optionally function in True IDE mode. The configuration of the CompactFlash Card shall be controlled using the standard PCMCIA PC Card configuration registers starting at address 200h in the Attribute Memory space of the storage card or for True IDE Mode, pin 9 being grounded. The configuration of the CF+ Card shall be controlled using configuration registers starting at the address defined in the Configuration Tuple (CISTPL_CONFIG) in the Attribute Memory space of the CF+ Card.

Table 5 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash Storage Card or CF+ Card sources are outputs. The CompactFlash Storage Card and CF+ Card logic levels conform to those specified in the PCMCIA Release 2.1 specification. In Table 5, each signal has three possible operating modes: 1) PC Card Memory, 2) PC Card I/O and 3) True IDE. True IDE mode is required for CompactFlash Storage cards, and optional for CF+ Cards. All outputs from the card are totempole except the data bus signals that are bi-directional tri-state. Refer to *Section* 4.3 for definitions of Input and Output type.

Table 4: Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3	27	D11[1]	I/O	I1Z, OZ3
28	D12[1]	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3	28	D12[1]	I/O	I1Z, OZ3
29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3	29	D13[1]	I/O	I1Z, OZ3
30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3	30	D14[1]	I/O	I1Z, OZ3
31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3	31	D15[1]	I/O	I1Z, OZ3
32	-CE2[1]	I	I3U	32	-CE2[1]	I	I3U	32	-CS1[1]	I	I3Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD HSTROBE[10] -HDMARDY[11]	I	I3U	34	-IORD HSTROBE[10] -HDMARDY[11]	I	I3U	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	I3Z

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
35	-IOWR	I	I3U	35	-IOWR	I	I3U	35	-IOWR[7]	I	I3Z
	STOP[10,11]				STOP[10,11]				STOP[8,9]		
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE[3]	I	I3U
37	READY	O	OT1	37	-IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL[5]	I	I2Z	39	-CSEL[5]	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY[7]	O	ON1
	-DDMARDY[10]				-DDMARDY[10]				-DDMARDY[8]		OT1[13]
	DSTROBE[11]				DSTROBE[11]				DSTROBE[9]		
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	DMARQ	O	OZ1
	-DMARQ [12]				-DMARQ [12]						
44	-REG	I	I3U	44	-REG	I	I3U	44	-DMACK [6]	I	I3U
	-DMACK [12]				DMACK [12]						
45	BVD2	O	OT1	45	-SPKR	O	OT1	45	-DASP	I/O	I1U, ON1
46	BVD1	O	OT1	46	-STSCHG	O	OT1	46	-PDIAG	I/O	I1U, ON1
47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3	47	D08[1]	I/O	I1Z, OZ3
48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3	48	D09[1]	I/O	I1Z, OZ3
49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3	49	D10[1]	I/O	I1Z, OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Note: 1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host.

4) The mode is optional for CF+ Cards, but required for CompactFlash Storage Cards.

5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition

7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.

8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.

9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

10) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Write is active.

11) Signal usage in PC Card I/O and Memory Mode when Ultra DMA mode protocol DMA Read is active.

12) Signal usage in PC Card I/O and Memory Mode when Ultra DMA protocol is active.

13) Signal is a totem-pole output during Ultra DMA data bursts in True IDE mode.

Table 5: Signal Description

Signal Name	Dir.	Pin	Description
A10 – A00 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
A10 – A00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A02 - A00 (True IDE Mode)	I	18,19,20	In True IDE Mode, only A[02:00] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 30, Table 33, Table 35, Table 39, Table 41 and Table 42. While (-) DMACK is asserted, -CE1 and -CE2 shall be held negated and the width of the transfers shall be 16 bits.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the address range select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.

Signal Name	Dir.	Pin	Description
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)	--	1,50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.

Signal Name	Dir.	Pin	Description
-INPACK (PC Card Memory Mode except Ultra DMA Protocol Active)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode except Ultra DMA Protocol Active) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU. Hosts that support a single socket per interface logic, such as for Advanced Timing Modes and Ultra DMA operation may ignore the –INPACK signal from the device and manage their input buffers based solely on Card Enable signals.
-DMARQ (PC Card Memory Mode - Ultra DMA Protocol Active) -DMARQ (PC Card I/O Mode - Ultra DMA Protocol Active) DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-)DMACK, i.e., the device shall wait until the host asserts (-)DMACK before negating (-)DMARQ, and re-asserting (-)DMARQ if there is more data to transfer. In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1)and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.

Signal Name	Dir.	Pin	Description
-IORD (PC Card Memory Mode except Ultra DMA Protocol Active)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode except Ultra DMA Protocol Active)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
-HDMARDY (All Modes - Ultra DMA Protocol DMA Read)			In all modes when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer.
HSTROBE (All Modes - Ultra DMA Protocol DMA Write)			In all modes when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode – Except Ultra DMA Protocol Active)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode – Except Ultra DMA Protocol Active)			In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
STOP (All Modes – Ultra DMA Protocol Active)			In All Modes, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA data burst.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.

Signal Name	Dir.	Pin	Description
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode – Except Ultra DMA Protocol Active) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. In PC Card Memory Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal negated during the execution of any DMA Command by the device.
-REG (PC Card I/O Mode – Except Ultra DMA Protocol Active)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. In PC Card I/O Mode, when Ultra DMA Protocol is supported by the host and the host has enabled Ultra DMA protocol on the card the, host shall keep the -REG signal asserted during the execution of any DMA Command by the device.
-DMACK (PC Card Memory Mode when Ultra DMA Protocol Active) DMACK (PC Card I/O Mode when Ultra DMA Protocol Active) -DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PC Card and True-IDE modes of operation need not alter the PC Card mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.

Signal Name	Dir.	Pin	Description
RESET (PC Card I/O Mode) -RESET (True IDE Mode)			This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	--	13,38	+5 V, +3.3 V power. This signal is the same for all modes. This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode – Except Ultra DMA Protocol Active) -WAIT (PC Card I/O Mode – Except Ultra DMA Protocol Active) IORDY (True IDE Mode – Except Ultra DMA Protocol Active) -DDMARDY (All Modes – Ultra DMA Write Protocol Active) DSTROBE (All Modes – Ultra DMA Read Protocol Active)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
-WE (PC Card Memory Mode) -WE (PC Card I/O Mode) -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.

Signal Name	Dir.	Pin	Description
WP (PC Card Memory Mode) Write Protect	O	24	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation – When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

4.3 Electrical Specification

Table 6, Table 7, Table 8, Table 9, and Table 12 define all D.C. Characteristics for the CompactFlash Storage Card and CF+ Card Series. Unless otherwise stated, conditions are:

Vcc = 5V ±10%

Vcc = 3.3V ± 5%

Ta = 0°C to 60°C

Table 6: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	Vcc	-0.3V min. to 6.5V max.
Voltage on any pin except Vcc with respect to GND.	V	-0.5V min. to Vcc + 0.5V max.

Table 7: Input Power

Voltage	Maximum Average RMS Current		Measurement Method
	Power Level 0	Power Level 1	
3.3V ± 5%	75 mA	500 mA	3.3V at 25°C
5.0V ± 10%	100 mA	500 mA	5.0V at 25°C

CompactFlash and CF+ products shall operate correctly in both voltage ranges as shown in Table 7: Input Power above. To comply with this specification, current requirements shall not exceed the maximum limit.

The maximum average RMS current for CompactFlash cards is 75 mA at 3.3V and 100 mA at 5V. For CF+ cards, two power levels are defined. Power Level 0 has the same current specifications as CompactFlash cards, while Power Level 1 has an increased maximum current of 500 mA for both 3.3V and 5V.

CF+ cards shall operate within the specifications for Power Level 0 at power on and after reset. CF+ cards shall also support CIS reads and (for ATA CF+ cards only) ATA Identify Device commands in Power Level 0. This requirement allows the host device to determine whether the CF+ card has commands, which require Power Level 1 (see *Sections* 5.2 and 6.2.1.6.31). If the host cannot support Power Level 1, the host can either disable Power Level 1 commands in the CF+ card (see *Sections* 4.4.5 and 6.2.1.29 or reject the CF+ card).

An example of a CF+ card using both Power Level 0 and Power Level 1 is a disk drive. Typically, commands that require the spindle to rotate (e.g., read/write commands) are Power Level 1 commands. CF+ disk drives shall make provisions to accommodate the execution of CIS reads and ATA Identify Device commands in Power Level 0; that is, without rotating the spindle.

Another class of CompactFlash card that can utilize Power Level 1 is the Power Enhanced CF Storage Card. These cards allow enhanced operation in Power Level 1, but do not require Power Level 1 for any function. The cards report their current power level in ID Drive Word 160. They shall support all mandatory commands and all implemented commands and protocols in both Power Level 0 and Power Level 1. These cards shall report identical supported features through the Identify Device command regardless of whether the command is issued in Power Level 0 or Power Level 1. The cards power up in Power Level 0 and remain in Power Level 0 until the host uses the Set Features command (see section 6.2.1.29) to control Power Level 1 operation. Hosts

shall use the Set Features command to enable and disable Power Level 1 in Power Enhanced CF Storage Cards.

4.3.1 Current Measurement

For Compact Flash Storage Cards, current measurement is accomplished by connecting an amp meter (set to the 2 amp scale range) with a fast current probe with an RC filter with a time constant of 0.1 msec, in series with the Vcc supply to the CompactFlash Storage Card. Current measurements are to be taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in the above Table 7: Input Power.

For CF+ cards, a fast (>1 MHz) current probe monitors current on the Vcc supply to the CF+ card. The output of the current probe is filtered by an RC filter with a time constant of 0.1 msec. The output of the filter is monitored with a fast (>1 MHz) scope or other monitor. The filtered output measured in this way shall not exceed the specifications shown for Power Level 0 (for all CF+ cards) and for Power Level 1 (for CF+ cards supporting Power Level 1).

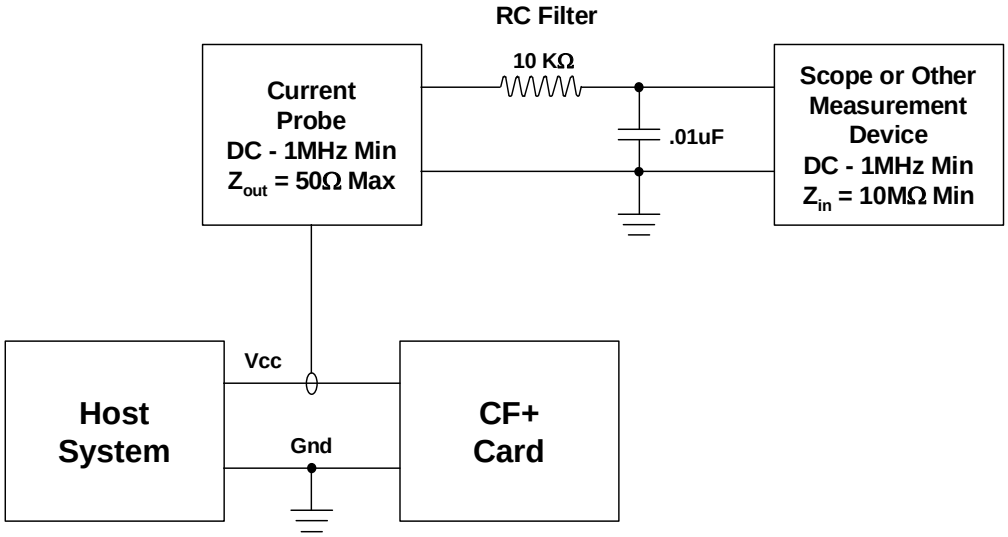


Figure 23: CF+ Power Supply Current Measurement Method

4.3.2 Input Leakage Current

Note: In Table 8 below, x refers to the characteristics described in *Section* 4.3.3. For example, I1U indicates a pull-up resistor with a type 1 input characteristic.

Table 8: Input Leakage Current

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
IxZ	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
IxU	Pull-Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull-Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

Note: The minimum pull-up resistor resistance meets the PCMCIA PC Card specification of 10k ohms but is intentionally higher in the CompactFlash Specification to reduce power use.

4.3.3 Input Characteristics

Table 9: Input Characteristics

Type	Parameter	Symbol	MIN	TYP	MAX	MIN	TYP	MAX	Units
			VCC = 3.3 V			VCC = 5.0 V			
1	Input Voltage CMOS	Vih Vil	2.4		 0.6	4.0 [1]		 0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		 0.6	2.0		 0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

Notes: 1) Per PCMCIA PC Card Electrical Specification Signal Interface Table 4-18 note 1, the host provides a logic output high voltage for a CMOS load of .9 x VCC. For a 5 volt product, this translates to .9 x 4.5 = 4.05 volts minimum Voh.

In UDMA modes greater than 4, the following characteristics apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 10: Input Characteristics (UDMA Mode > 4)

Parameter	Symbol	MIN	MAX	Units
DC supply voltage to receivers	V_{DD3}	3.3 - 8%	3.3 + 8%	Volts
Low to high input threshold	V+	1.5	2.0	Volts
High to low input threshold	V–	1.0	1.5	Volts
Difference between input thresholds: $((V+_{current\ value}) - (V-_{current\ value}))$	V_{HYS}	320		mV
Average of thresholds: $((V+_{current\ value}) + (V-_{current\ value}))/2$	V_{THRAVG}	1.3	1.7	Volts

4.3.4 Output Drive Type

Note: In Table 11 below, x refers to the characteristics described in *Section* 4.3.5. For example, OT3 refers to Totempole output with a type 3 output drive characteristic.

Table 11: Output Drive Type

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

4.3.5 Output Drive Characteristics

Table 12: Output Drive Characteristics

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
2	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

In UDMA modes greater than 4, the characteristics specified in the following table apply. Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 13: Output Drive Characteristics (UDMA Mode > 4)

Parameter	Symbol	MIN	MAX	Units
DC supply voltage to drivers	V_{DD3}	3.3 - 8%	3.3 + 8%	Volts
Voltage output high at -6 mA to +3 mA (at V_{oH2} the output shall be able to supply and sink current to V_{DD3})	V_{oH2}	VDD_3 - 0.51	VDD_3 + 0.3	Volts
Voltage output low at 6 mA	V_{oL2}		0.51	Volts

Notes:

1) I_{oLDASP} shall be 12 mA minimum to meet legacy timing and signal integrity.

2) I_{oH} value at 400 µA is insufficient in the case of DMARQ that is pulled low by a 5.6 kΩ resistor.

3) Voltage output high and low values shall be met at the source connector to include the effect of series termination.

4) A device shall have less than 64 µA of leakage current into a 6.2 KΩ pull-down resistor while the INTRQ signal is in the released state.

4.3.6 Signal Interface

Electrical specifications shall be maintained to ensure data reliability. Additional requirements are necessary for Advanced Timing Modes and Ultra DMA modes operations. See sections 4.3.7 and 4.3.8 for additional information.

Table 14: Electrical Interface

Item	Signal	Card [10]	Host [10]
Control Signal	-CE1 -CE2 -REG -IORD -IOWR	Pull-up to Vcc 500 KΩ ≥ R ≥ 50 KΩ and shall be sufficient to keep inputs inactive when the pins are not connected at the host. [1]	
	-OE -WE	Pull-up to Vcc 500 KΩ ≥ R ≥ 50 KΩ. [1, 2]	
	RESET	Pull-up to Vcc 500 KΩ ≥ R ≥ 50 KΩ. [1, 2,9]	
Status Signal	READY -WAIT WP		Pull-up to Vcc R ≥ 10 KΩ. [3]
	-INPACK		In PCMCIA PC Card modes Pull-up to Vcc R ≥ 10 KΩ. [4] In True IDE mode, if DMA operation is supported by the host, Pull-down to Gnd R ≥ 5.6 KΩ. [5] PC Card / True IDE hosts switch the pull-up to pull-down in True IDE mode if DMA operation is supported. The PC Card mode Pull-up may be left active during True IDE mode if True IDE DMA operation is not supported.
Address	A[10:00] -CSEL		
Data Bus	D[15:00]		[1,]
Card Detect	-CD[2:1]	Connected to GND in the card	
Voltage Sense	-VS1 -VS2		Pull-up to Vcc 10 KΩ ≤ R ≤ 100KΩ.
Battery/Detect	BVD[2:1]		Pull-up R ≥ 50 KΩ. [3, 6]

Notes: 1) Control Signals: each card shall present a load to the socket no larger than 50 pF [10] at a DC current of 700 μA low state and 150 μA high state, including pull-resistor. The socket shall be able to drive at least the following load [10] while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (50 pF with DC current 700 μA low state and 150 μA high state per socket).

2) Resistor is optional.

3) Status Signals: the socket shall present a load to the card no larger than 50 pF [10] at a DC current of 400 μA low state and 100 μA high state, including pull-up resistor. The card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 50 pF at a DC current of 400 μA low state and 100 μA high state.

4) Status Signals: the socket shall present a load to the card no larger than 50 pF [10] at a DC current of 400 μA low state and 100 μA high state, including pull-up resistor. The card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 50 pF at a DC current of 400 μA low state and 100 μA high state.

5) Status Signals: the socket shall present a load to the card no larger than 50 pF [10] at a DC current of 400 μA low state and 100 μA high state, including pull-up resistor. The card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 50 pF at a DC current of 400 μA low state and 1100 μA high state.

6) BVD2 was not defined in the JEIDA 3.0 release. Systems fully supporting JEIDA release 3 SRAM cards shall pull-up pin 45 (BVD2) to avoid sensing their batteries as "Low."

7) Address Signals: each card shall present a load of no more than 100pF [10] at a DC current of 450μA low state and 150μA high state. The host shall be able to drive at least the following load [10] while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (100pF with DC current 450μA low state and 150μA high state per socket).

8) Data Signals: the host and each card shall present a load no larger than 50pF [10] at a DC current of 450μA and 150μA high state. The host and each card shall be able to drive at least the following load [10] while meeting all AC timing requirements: 100pF with DC current 1.6mA low state and 300μA high state. This permits the host to wire two sockets in parallel without derating the card access speeds.

9) Reset Signal: This signal is pulled up to prevent the input from floating when a CFA to PCMCIA PC Card adapter is used in a PCMCIA revision 1 host. However, to minimize DC current drain through the pull-up resistor in normal operation the pull-up should be turned off once the Reset signal has been actively driven low by the host. Consequently, the input is specified as an I2Z because the resistor is not necessarily detectable in the input current leakage test.

10) Host and card restrictions for CF Advanced Timing Modes and Ultra DMA modes: See section 4.3.7: Additional Requirements for CF Advanced Timing Modes and section 4.3.8: Ultra DMA Electrical Requirements for additional required limitations on the implementation of CF Advanced Timing modes and Ultra DMA modes respectively.

4.3.7 Additional Requirements for CF Advanced Timing Modes

The CF Advanced Timing modes include PC Card I/O and Memory modes that are 100ns or faster, PC Card Ultra DMA modes 3 or above and True IDE PIO Modes 5,6, Multiword DMA Modes 3,4 and True IDE Ultra DMA modes 3 or above.

When operating in CF Advanced timing modes, the host shall conform to the following requirements:

1) Only one CF device shall be attached to the CF Bus.

2) The host shall not present a load of more than 40pF to the device for all signals, including any cabling.

3) The maximum cable length is 0.15 m (6 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are ***not*** supported.

4) The -WAIT and IORDY signals shall be ignored by the host.

Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes

4.3.8 Ultra DMA Electrical Requirements

Operation in Ultra DMA mode requires careful attention to cabling, printed circuit board (PCB) trace routing and termination for reliable operation. These requirements are described in the following sections. Both PC Card and True IDE Ultra DMA modes 3 and above are also restricted by the requirements of section 4.3.7 Additional Requirements for CF Advanced Timing Modes.

4.3.8.1 Host and Card signal capacitance limits for Ultra DMA operation

The host interface signal capacitance at the host connector shall be a maximum of 25 pF for each signal as measured at 1 MHz.

The card interface signal capacitance at the card connector shall be a maximum of 20 pF for each signal as measured at 1 MHz.

4.3.8.2 Series termination required for Ultra DMA operation

Series termination resistors are required at both the host and the card for operation in any of the Ultra DMA modes. Table 15 describes typical values for series termination at the host and the device

Table 15: Typical Series Termination for Ultra DMA

Signal	Host Termination	Device Termination
-IORD (-HDMARDY, HSTROBE)	22 ohm	82 ohm
-IOWR (STOP)	22 ohm	82 ohm
-CS0, -CS1	33 ohm	82 ohm
A00, A01, A02	33 ohm	82 ohm
-DMACK	22 ohm	82 ohm
D15 through D00	33 ohm	33 ohm
DMARQ	82 ohm	22 ohm
INTRQ	82 ohm	22 ohm
IORDY (-DDMARDY, DSTROBE)	82 ohm	22 ohm
-RESET	33 ohm	82 ohm
NOTE – Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. shows signals also requiring a pull-up or pull-down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.		

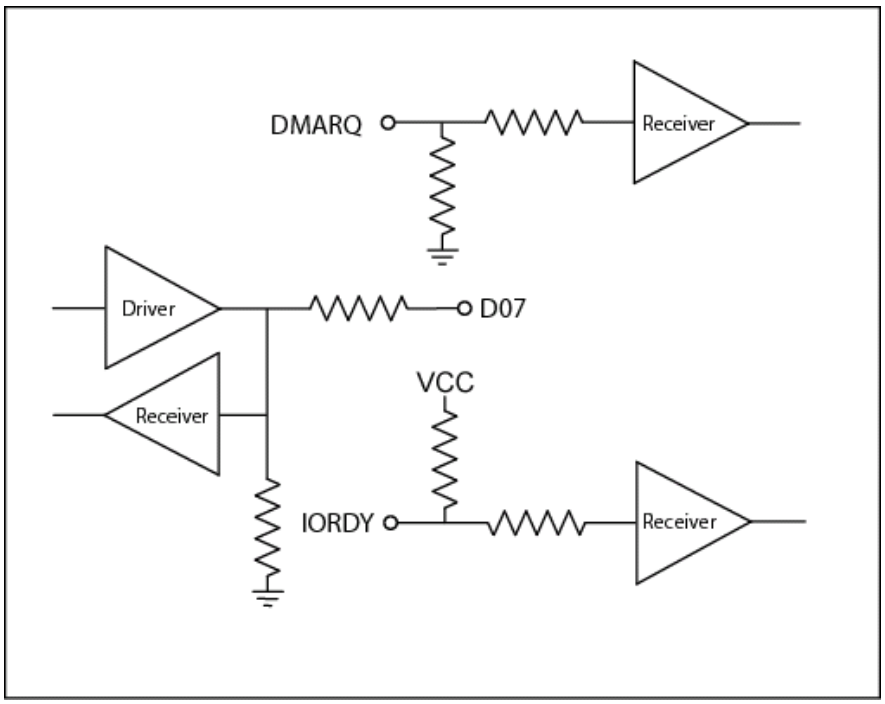


Figure 24: Ultra DMA Termination with Pull-up or Pull down Example

4.3.8.3 Printed Circuit Board (PCB) Trace Requirements for Ultra DMA

On any PCB for a host or device supporting Ultra DMA:

- The longest D[15:00] trace shall be no more than 0.5" longer than either STROBE trace as measured from the IC pin to the connector.
- The shortest D[15:00] trace shall be no more than 0.5" shorter than either STROBE trace as measured from the IC pin to the connector.

4.3.8.4 Ultra DMA Mode Cabling Requirement

Operation in Ultra DMA mode requires a crosstalk suppressing cable. The cable shall have a grounded line between each signal line.

For True IDE mode operation using a cable with IDE (ATA) type 40 pin connectors it is recommended that the host sense the cable type using the method described in the ANSI INCITS 361-2002 AT Attachment - 6 standard, to prevent use of Ultra DMA with a 40 conductor cable.

4.3.9 Interface/Bus Timing

There are two types of bus cycles and timing sequences that occur in the PC Card type interface, direct mapped I/O transfer and memory access. The two timing sequences are detailed in the PCMCIA PC Card Standard. The CompactFlash Storage Card and CF+ Card conform to the timing in that reference document.

4.3.10 Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300 ns. Detailed timing specs are shown in Table 16.

Table 16: Attribute Memory Read Timing

Speed Version			300 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.

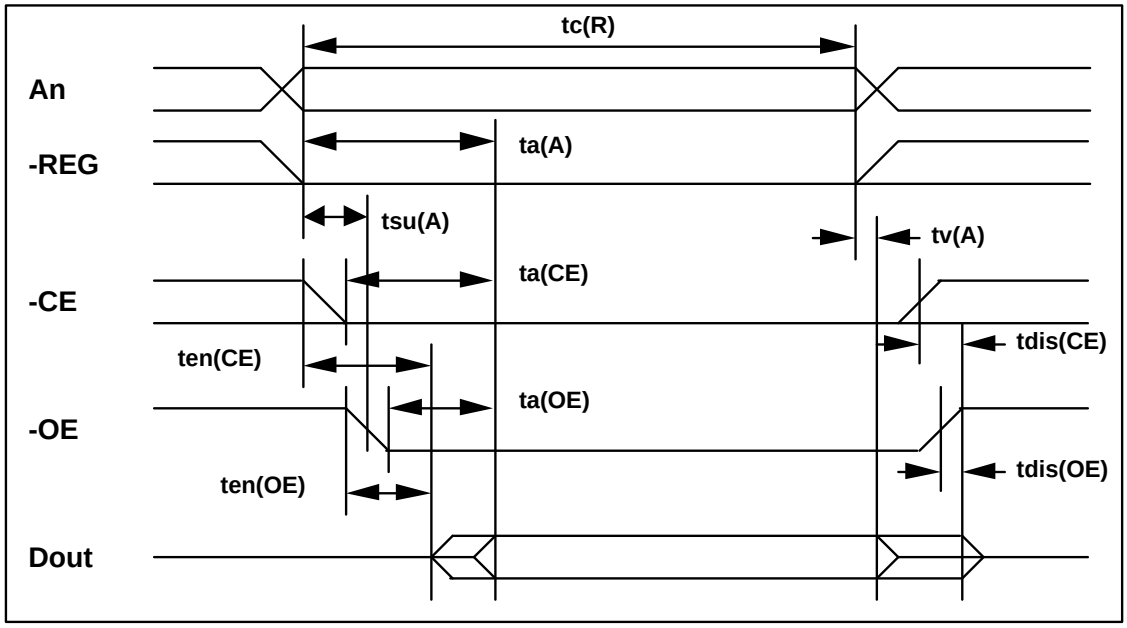


Figure 25: Attribute Memory Read Timing Diagram

4.3.11 Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250 ns. Detailed timing specifications are shown in Table 17.

Table 17: Configuration Register (Attribute Memory) Write Timing

Speed Version			250 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns**	**Max ns**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card.

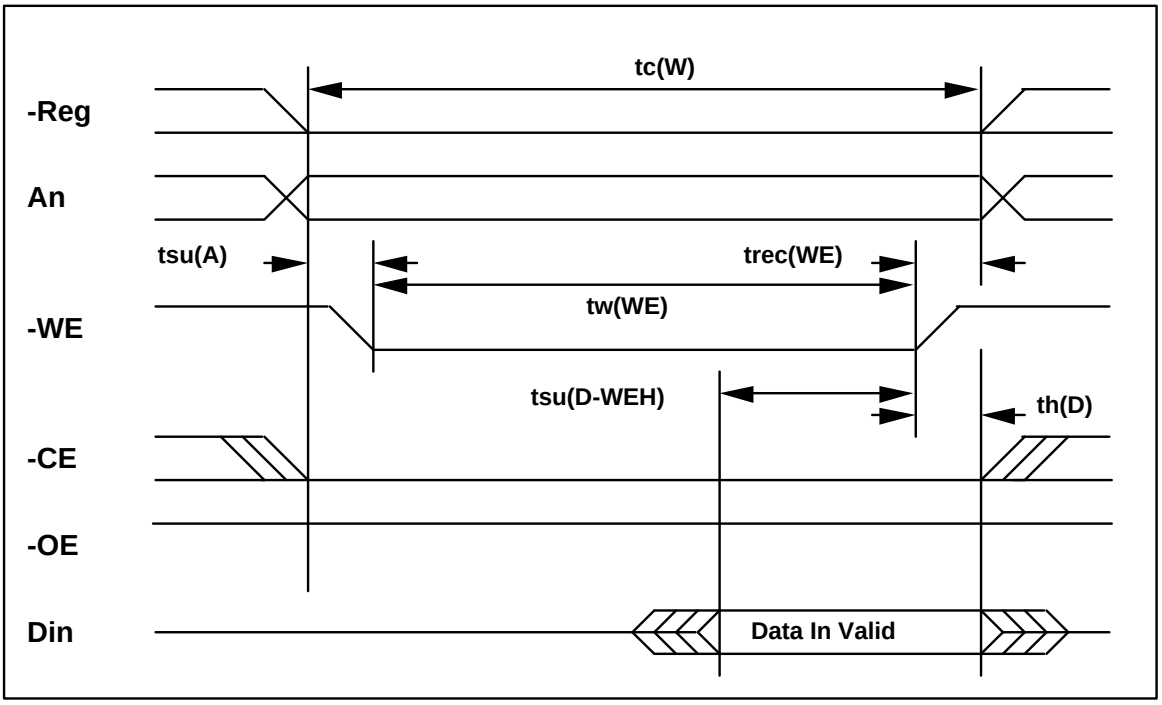


Figure 26: Configuration Register (Attribute Memory) Write Timing Diagram

4.3.12 Common Memory Read Timing Specification

Table 18: Common Memory Read Timing

	Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[1]

Notes: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA PC Card specification of 12µs but is intentionally less in this specification.

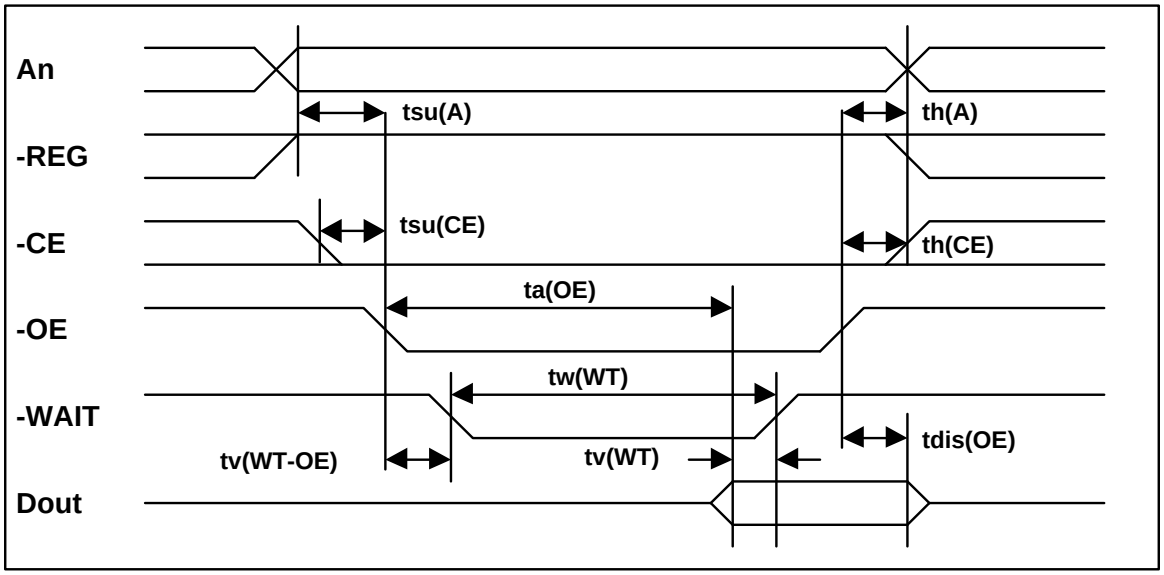


Figure 27: Common Memory Read Timing Diagram

4.3.13 Common Memory Write Timing Specification

Table 19: Common Memory Write Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35		35		35		na[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw (WT)	tWTLWTH		350 (3000 for *CF*+)		350 (3000 for *CF*+)		350 (3000 for *CF*+)		na[1]

Notes: 1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA PC Card specification of 12µs but is intentionally less in this specification.

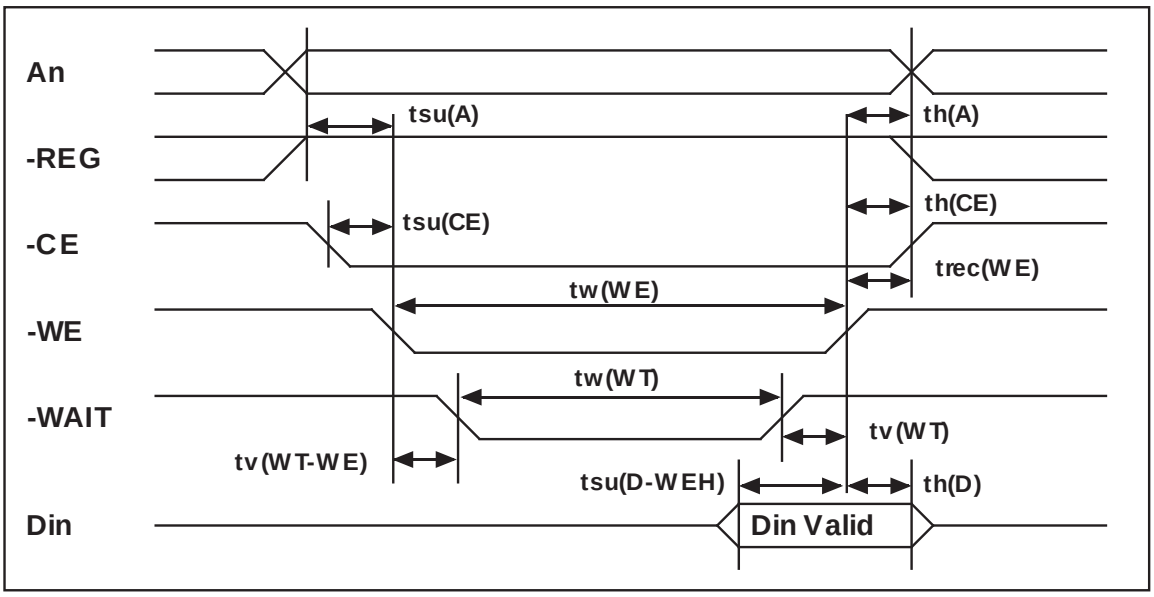


Figure 28: Common Memory Write Timing Diagram

4.3.14 I/O Input (Read) Timing Specification

Table 20: I/O Read Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG (IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG (IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINPACK (IORD)	tIGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK (IORD)	tIGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tIGLWTL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		na[2]
Wait Width Time[3]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA PC Card specification of 12µs but is intentionally less in this spec.

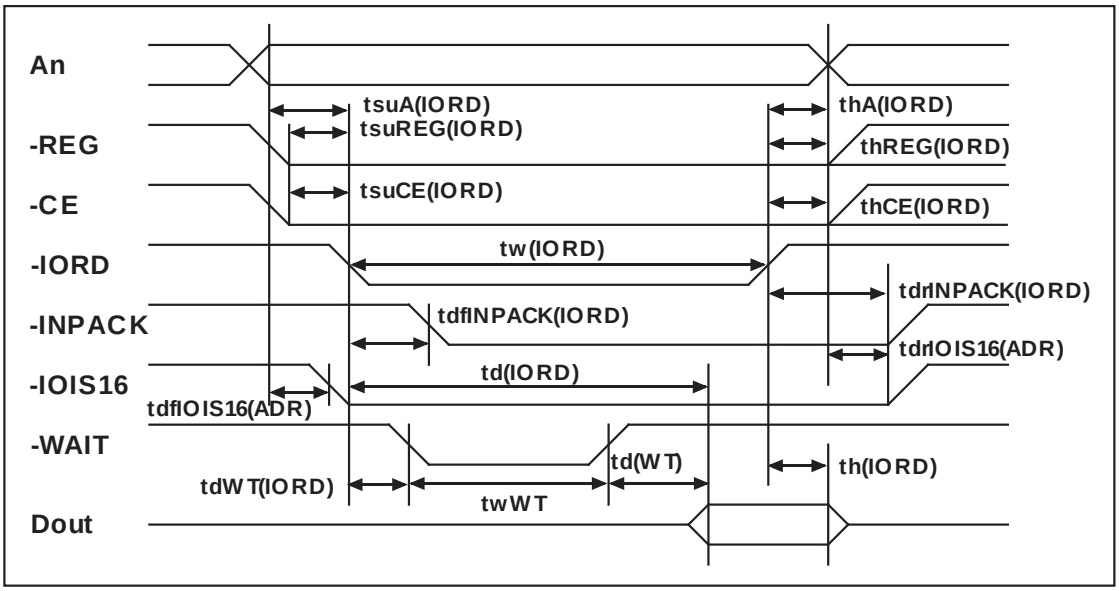


Figure 29: I/O Read Timing Diagram

4.3.15 I/O Output (Write) Timing Specification

Table 21: I/O Write Timing

Cycle Time Mode:			255 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG (IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOWR[3]	tdWT(IOWR)	tIWLWTL		35		35		35		na[2]
IOWR high from Wait high[3]	tdrIOWR (WT)	tWTJIWH	0		0		0		na[2]	
Wait Width Time[3]	tw(WT)	tWTLWTH		350 (3000 for *CF+*)		350 (3000 for *CF+*)		350 (3000 for *CF+*)		na[2]

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA PC Card specification of 12 µs but is intentionally less in this specification.

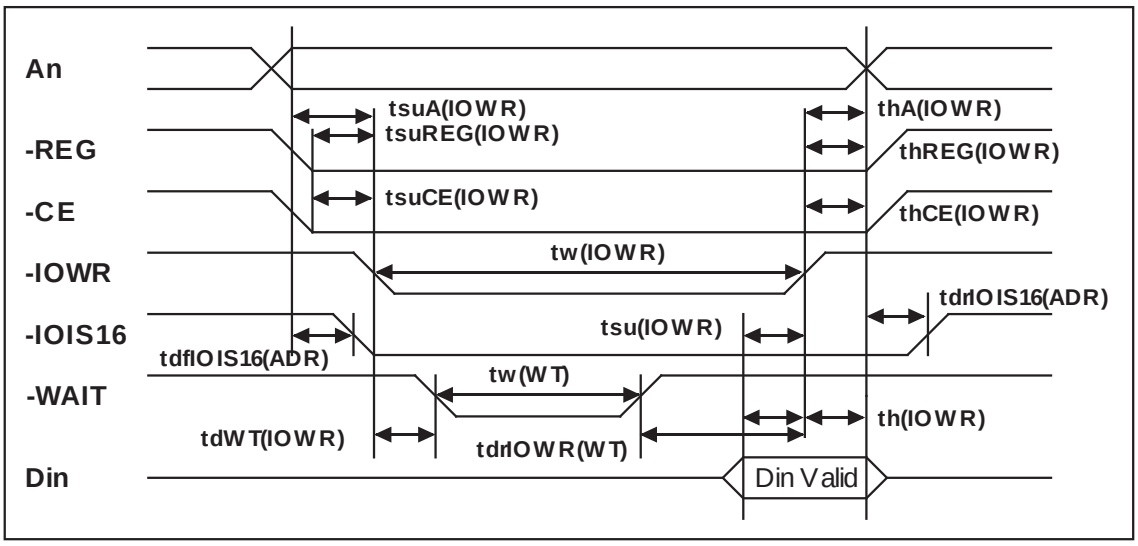


Figure 30: I/O Write Timing Diagram

4.3.16 True IDE PIO Mode Read/Write Timing Specification

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA PC Card specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 22: True IDE PIO Mode Read/Write Timing

	Item	Mode							Note
		0	1	2	3	4	5	6	
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	1
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	1
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
T6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	4
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]	

Notes: All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

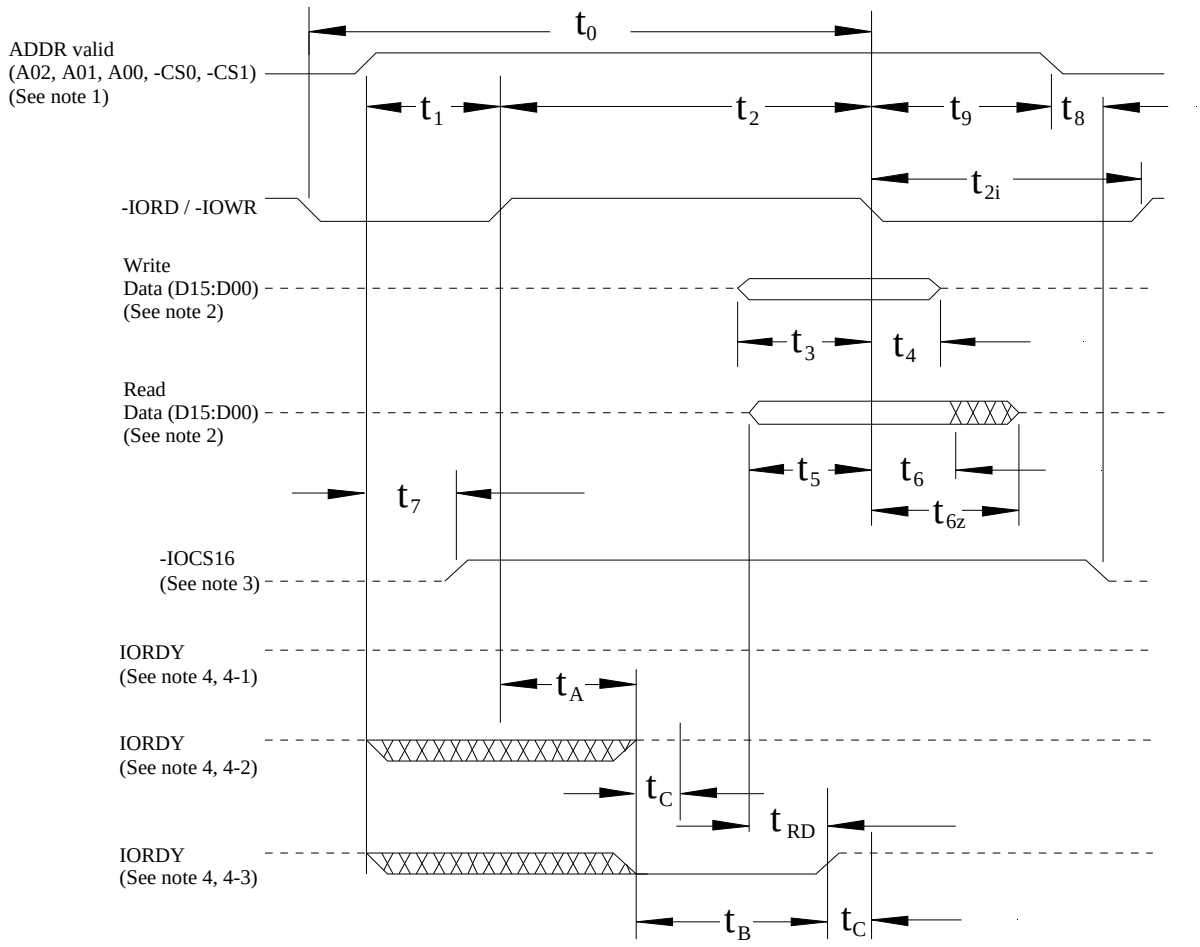
1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).

3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.



Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 31: True IDE PIO Mode Timing Diagram

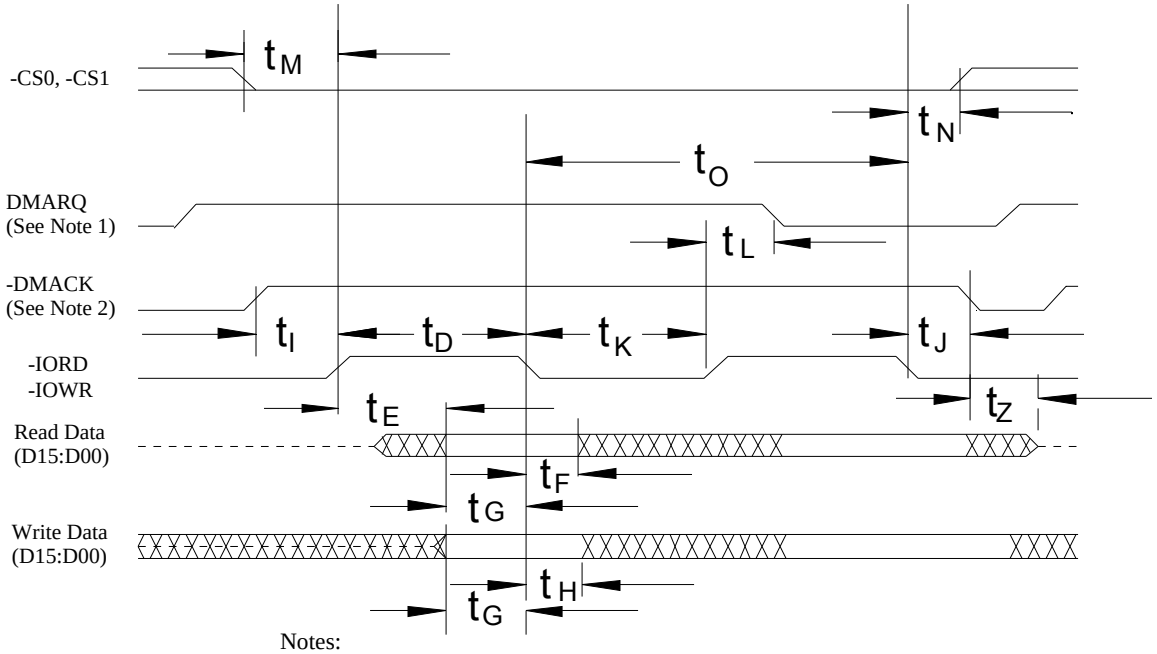
4.3.17 True IDE Multiword DMA Mode Read/Write Timing Specification

The timing diagram for True IDE DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA PC Card specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

Table 23: True IDE Multiword DMA Mode Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55	1
t_E	-IORD data access (max)	150	60	50	50	45	
t_F	-IORD data hold (min)	5	5	5	5	5	
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10	
t_H	-IOWR data hold (min)	20	15	10	5	5	
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0	
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	25	20	1
t_{KW}	-IOWR negated width (min)	215	50	25	25	20	1
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35	
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5	
t_N	CS(1:0) hold	15	10	10	10	10	
t_Z	-DMACK	20	25	25	25	25	

Notes: 1) t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, $t_{D,}$ t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and $t_{KR\ or}$ t_{KW}.for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.



Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

(2) This signal may be negated by the host to suspend the DMA transfer in progress.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Figure 32: True IDE Multiword DMA Mode Read/Write Timing Diagram

4.3.18 Ultra DMA Mode Read/Write Timing Specification

4.3.18.1 Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).

Ultra DMA operations can take place in any of the three basic interface modes: PC Card Memory mode, PC Card I/O mode, and True IDE (the original mode to support UDMA). The usage of signals in each of the modes is shown in Table 24:Ultra DMA Signal Usage In Each Interface Mode

Table 24:Ultra DMA Signal Usage In Each Interface Mode

UDMA Signal	Type	Pin # (Non UDMA MEM MODE)	PC CARD MEM MODE UDMA	PC CARD IO MODE UDMA	TRUE IDE MODE UDMA
DMARQ	Output	43 (-INPACK)	-DMARQ	-DMARQ	DMARQ
DMACK	Input	44 (-REG)	-DMACK	DMACK	-DMACK
STOP	Input	35 (-IOWR)	STOP [1]	STOP [1]	STOP [1]
HDMARDY(R) HSTROBE(W)	Input	34 (-IORD)	-HDMARDY(R) [1, 2] HSTROBE(W) [1, 3, 4]	-HDMARDY(R) [1, 2] HSTROBE(W) [1, 3, 4]	-HDMARDY(R) [1, 2] HSTROBE(W) [1, 3, 4]
DDMARDY(W) DSTROBE(R)	Output	42 (-WAIT)	-DDMARDY(W) [1, 3] DSTROBE(R) [1. 2. 4]	-DDMARDY(W) [1, 3] DSTROBE(R) [1. 2. 4]	-DDMARDY(W) [1, 3] DSTROBE(R) [1. 2. 4]
DATA	Bidir	… (D[15:00])	D[15:00]	D[15:00]	D[15:00]
ADDRESS	Input	… (A[10:00])	A[10:00]	A[10:00]	A[02:00] [5]
CSEL	Input	39 (-CSEL)	-CSEL	-CSEL	-CSEL
INTRQ	Output	37 (READY)	READY	-INTRQ	INTRQ
Card Select	Input	7 (-CE1) 31 (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes: 1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.

2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.

3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.

4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.

5) Address lines 03 through 10 are not used in True IDE mode.

Several signal lines are redefined to provide different functions during an Ultra DMA data burst. These lines assume their UDMA definitions when:

1. an Ultra DMA mode is selected, and
2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and
3. the device asserts (-)DMARQ, and
4. the host asserts (-)DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA data burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA data burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA data burst. At the end of an Ultra DMA data burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE – If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

4.3.18.2 Restrictions and Considerations During Ultra DMA Commands

There are number of important restrictions and considerations for the implementation and use of Ultra DMA commands in CompactFlash devices. These are highlighted in the subsections below. Additional restrictions on specific modes of operation are given in sections 4.3.7: Additional Requirements for CF Advanced Timing Modes and 4.3.18.3: Specific rules for PC Card Memory Mode Ultra DMA.

4.3.18.2.1 System Restrictions for Ultra DMA modes 3 and above

Ultra DMA modes 3 and above are valid only for systems that meet the requirements of section 4.3.7 Additional Requirements for CF Advanced Timing Modes

4.3.18.2.2 UDMA Address and Card Enable Signals

The Card Enable signals (-CE1 / -CS0 and -CE2 / -CS1) shall remain negated during Ultra DMA data bursts.

The Address bus (A[10:00]) shall not transition unnecessarily during the UDMA command and shall remain fixed during an Ultra DMA data burst. In True IDE mode, the address lines (A[02:00]) shall be held to all zeros. This will reduce unnecessary noise during the UDMA command.

4.3.18.2.3 Task File registers shall not be written during an Ultra DMA command

The task file registers shall not be written after an Ultra DMA command is issued by the host and before the command completes. Writing to the device control register is permitted between bursts, but is expected to occur only to reset the card after an unrecoverable protocol error.

4.3.18.2.4 Ultra DMA transfers shall be 16 bits wide

All transfers during an Ultra DMA data burst are 16 bit wide transfers. The Set Features command that controls the bus width for PIO transfers does not affect the width of Ultra DMA transfers.

4.3.18.2.5 No Access to Memory or I/O Space during an Ultra DMA Data Burst

No access to common or attribute memory or to I/O space on the device is permitted during an Ultra DMA data burst.

4.3.18.3 Specific rules for PC Card Memory Mode Ultra DMA

In addition to the general restrictions for all Ultra DMA operations, these additional considerations exist for PC Card Memory Mode Ultra DMA operations.

4.3.18.3.1 No Access to Attribute Memory during PC Card Memory Mode DMA Commands

The host shall not attempt to access Attribute Memory space during a PC Card Memory Mode DMA command either before, between or within Ultra DMA data bursts.

4.3.18.3.2 READY signal handling during DMA commands in PC Card Memory Mode

In PC Card Memory Mode, the READY signal shall be negated (made BUSY) by the device upon receipt of a DMA command and shall remain negated until the command has completed at which time it shall be re-asserted.

This treatment allows the host to receive a single interrupt at the end of the command and avoids the extra overhead that would be associated with processing busy to ready transitions for each sector transferred as is the case when the READY toggles at the end of every sector of PIO Memory Mode transfers.

The BSY bit in the status register is permitted to be negated in the status register at any time that the DRQ bit in the status register is asserted. The only restriction is that either DRQ or BSY or both must remain asserted while the command is in progress.

4.3.18.4 Ultra DMA Phases of Operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA data burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA data burst termination phase. In addition, an Ultra DMA data burst may be paused during the data transfer phase (see: 14.3.18.5 Ultra DMA Data Transfer, for the detailed protocol descriptions for each of these phases. Table 25: Ultra DMA Data Burst Timing Requirements and Table 26: Ultra DMA Data Burst Timing Descriptions define the specific timing requirements). In the following rules -DMARDY is used in cases that could apply to either -DDMARDY or -HDMARDY, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

1. An Ultra DMA data burst is defined as the period from an assertion of (-)DMACK by the host during the assertion of (-)DMARQ by the device to the subsequent negation of (-)DMACK.

2. When operating in Ultra DMA modes 2, 1, or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA data burst is paused. When operating in Ultra DMA modes 6, 5, 4, or 3 a recipient shall be prepared to receive up to three data words whenever an Ultra DMA data burst is paused.

4.3.18.4.1 Ultra DMA Data Burst Initiation Phase Rules

1. An Ultra DMA data burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.

2. An Ultra DMA data burst shall always be requested by a device asserting DMARQ.

3. When ready to initiate the requested Ultra DMA data burst, the host shall respond by asserting -DMACK.

4. A host shall never assert -DMACK without first detecting that DMARQ is asserted.

5. For Ultra DMA data-in bursts: a device may begin driving D[15:00] after detecting that -DMACK is asserted, STOP negated, and -HDMARDY is asserted.

6. After asserting DMARQ or asserting -DDMARDY for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.

7. After negating STOP or asserting -HDMARDY for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

4.3.18.4.2 Ultra DMA Data transfer phase rules

1. The data transfer phase is in effect from after Ultra DMA data burst initiation until Ultra DMA data burst termination.

2. A recipient pauses an Ultra DMA data burst by negating -DMARDY and resumes an Ultra DMA data burst by reasserting -DMARDY.

3. A sender pauses an Ultra DMA data burst by not generating STROBE edges and resumes by generating STROBE edges.

4. A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate -DMARDY and wait the required period before signaling a termination request.

5. A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

4.3.18.4.3 Ultra DMA Data Burst Termination Phase Rules

1. Either a sender or a recipient may terminate an Ultra DMA data burst.

2. Ultra DMA data burst termination is not the same as command completion. If an Ultra DMA data burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA data burst at some later time or aborted by the host issuing a hardware or software reset or DEVICE RESET command if implemented by the device.

3. An Ultra DMA data burst shall be paused before a recipient requests a termination.

4. A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.

5. A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.

6. Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.

7. A sender shall return STROBE to the asserted state whenever the sender detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.

8. Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA data burst.

9. A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

4.3.18.5 Ultra DMA Data Transfers Timing

Table 25 and Table 26 define the timings associated with all phases of Ultra DMA data bursts.

Table 25: Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		UDMA Mode 6		Measure location
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	(see Note 2)
$t_{2CYCTYP}$	240		160		120		90		60		40		30		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		Note 3
t_{2CYC}	230		153		115		86		57		38		29		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		Sender
t_{FS}		230		200		170		130		120		90		80	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	Note 4
t_{MLI}	20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		Sender

Notes: All Timings in ns

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and -DMARDY transitions are measured at the sender connector.

3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5) The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

6) See the AC Timing requirements in Table 28: Ultra DMA AC Signal Requirements.

Table 26: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	6
t_{ZIORDY}	Minimum time before driving IORDY	4, 6
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes: 1) The parameters t_{UI}, t_{MLI} (in Figure 36: Ultra DMA Data-In Burst Device Termination Timing and Figure 37: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks,

i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

2) 80-conductor cabling (see 4.3.8.4) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4) For all timing modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5) The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

6) This parameter applies to True IDE mode operation only.

Table 27: Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)		UDMA Mode 5 (ns)		UDMA Mode6 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3		2.3	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0		5.2	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0		5.2	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)													
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)													
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)													
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)													

Notes: 1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.

2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).

3) The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Table 28: Ultra DMA AC Signal Requirements

Name	**Comment**	**Min [V/ns]**	**Max [V/ns]**	**Notes**
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Note: 1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled V_{OH} level with data transitions at least 120 nsec apart. The settled V_{OH} level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

4.3.18.5.1 Initiating an Ultra DMA Data-In Burst

a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 33: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:

c) The host shall keep -DMACK in the negated state before an Ultra DMA data burst is initiated.

d) The device shall assert DMARQ to initiate an Ultra DMA data burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

e) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

f) The host shall negate -HDMARDY.

g) In True IDE mode, the host shall not assert -CS0, -CS1 and A[02:00]. In PC Card modes, the host shall not assert -CE2, -CE1 and shall hold A[10:00] fixed until after negating -DMACK at the end of the burst.

h) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA data burst.

i) The host shall release D[15:00] within t_{AZ} after asserting -DMACK.

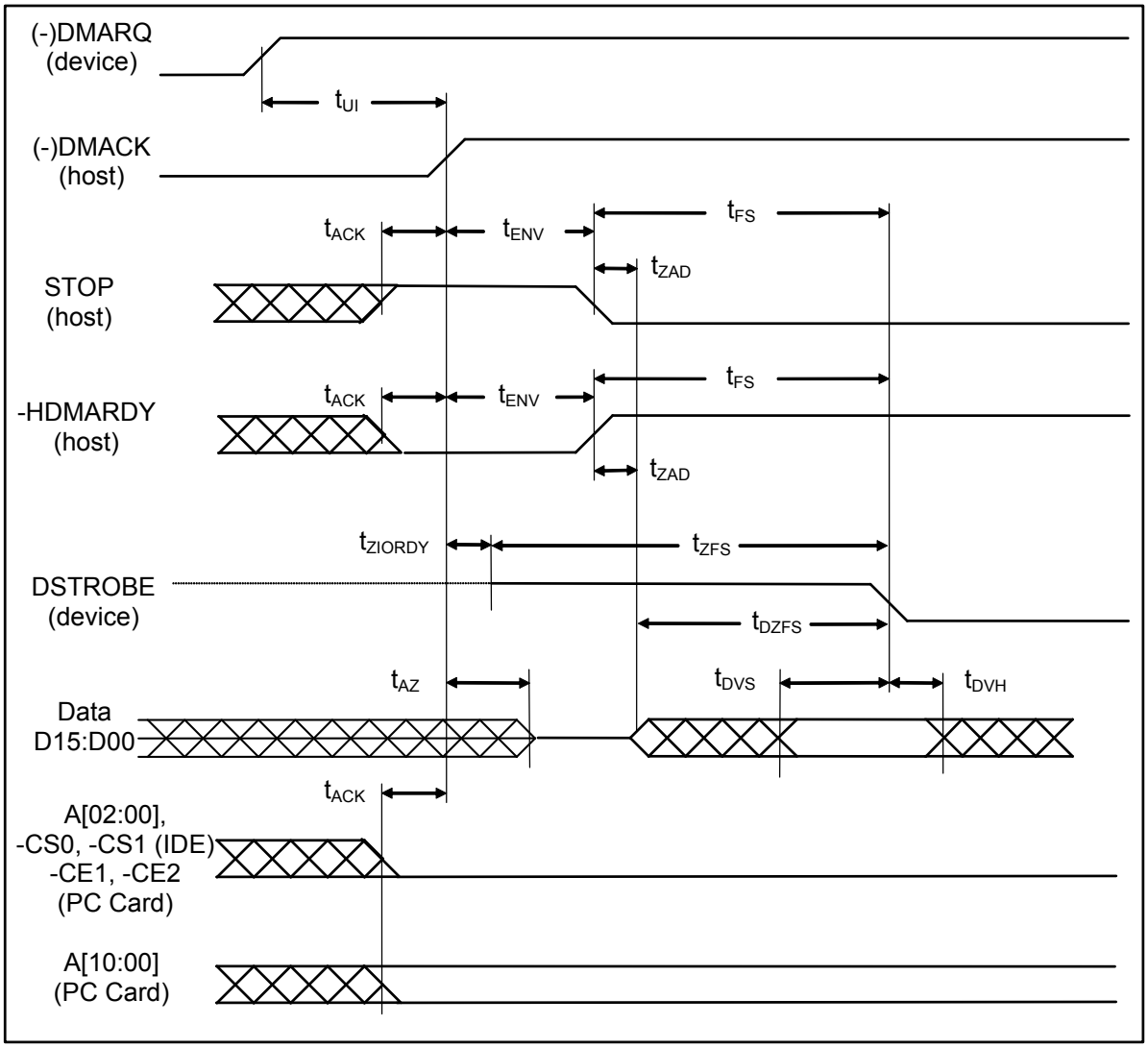
j) The device may assert DSTROBE t_{ZIORDY} after the host has asserted -DMACK. While operating in True IDE mode, once the device has driven DSTROBE, the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA data burst.

k) The host shall negate STOP and assert -HDMARDY within t_{ENV} after asserting -DMACK. After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).

l) The device shall drive D[15:00] no sooner than t_{ZAD} after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY.

m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j).

n) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto D[15:00].



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signals. The Bus polarity of (-)DMACK and (-)DMARQ are dependent on interface mode active.

Figure 33: Ultra DMA Data-In Burst Initiation Timing

4.3.18.5.2 Sustaining an Ultra DMA Data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 34: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

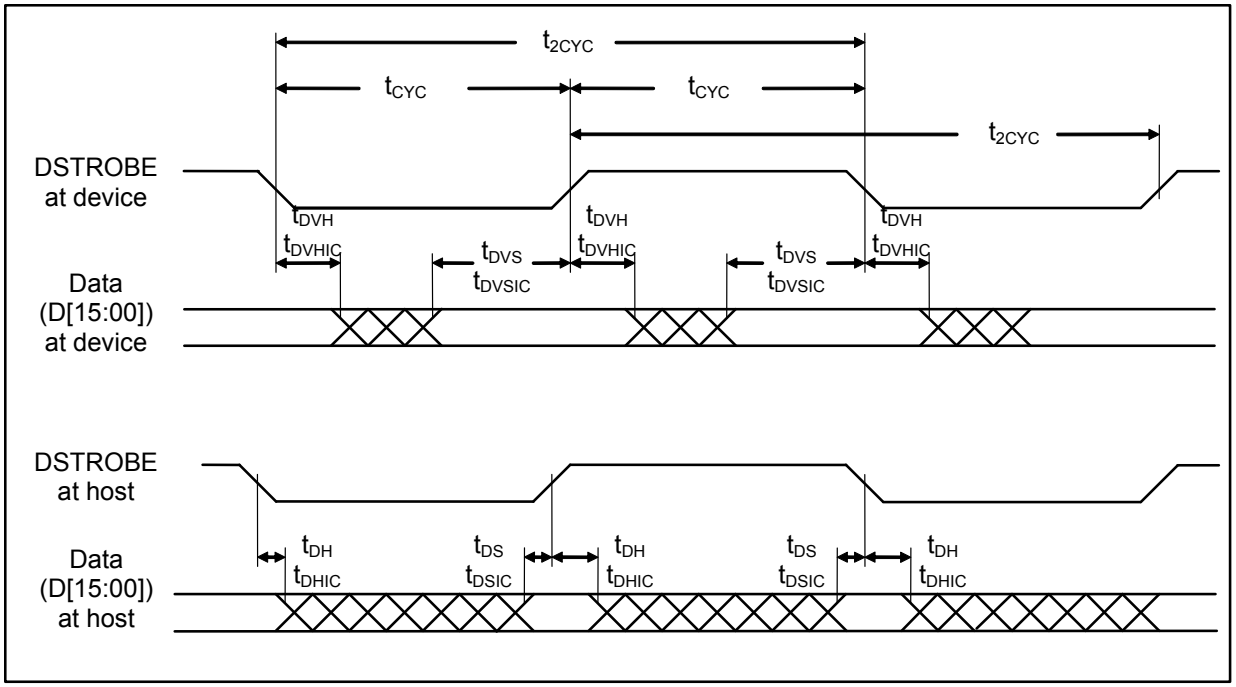
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall drive a data word onto D[15:00].

b) The device shall generate a DSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c) The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data.

d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA data burst is paused, whichever occurs first.



Notes: **D[15:00]** and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 34: Sustained Ultra DMA Data-In Burst Timing

4.3.18.5.3 Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 35: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in

Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

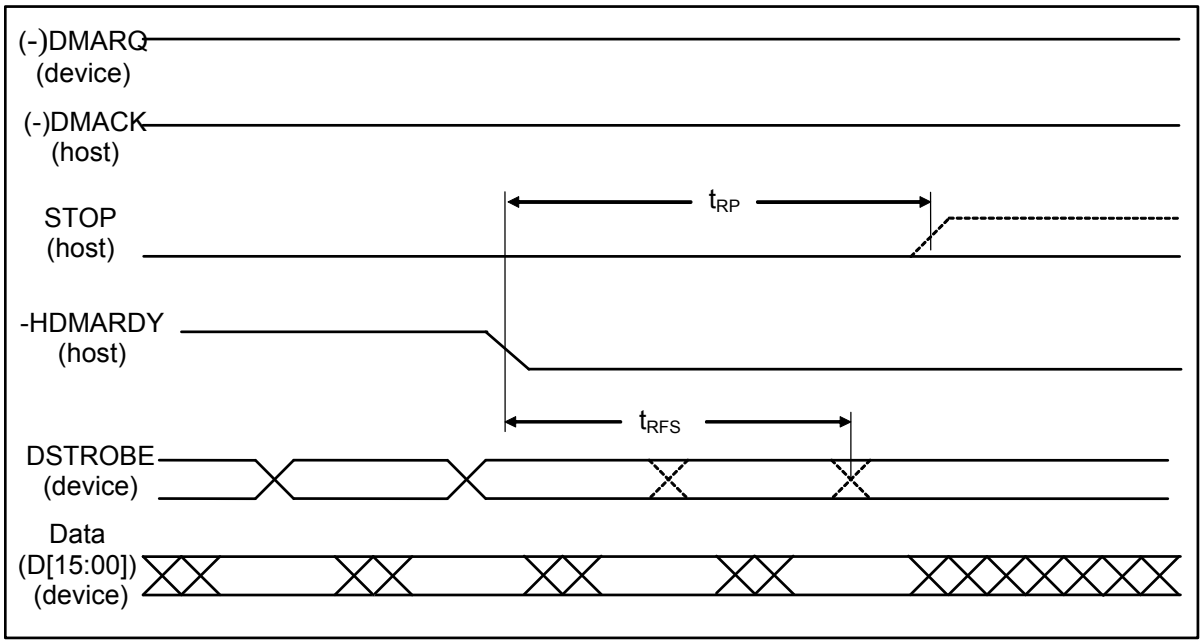
a) The host shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred.

b) The host shall pause an Ultra DMA data burst by negating -HDMARDY.

c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY.

d) While operating in Ultra DMA modes 2, 1, or 0 the host shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The host shall resume an Ultra DMA data burst by asserting -HDMARDY.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: 1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than t_{RP} after -HDMARDY is negated.

2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

3) The bus polarity of the (-) DMARQ and (-)DMACK signals is dependent on the active interface mode.

Figure 35: Ultra DMA Data-In Burst Host Pause Timing

4.3.18.5.4 Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 36: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

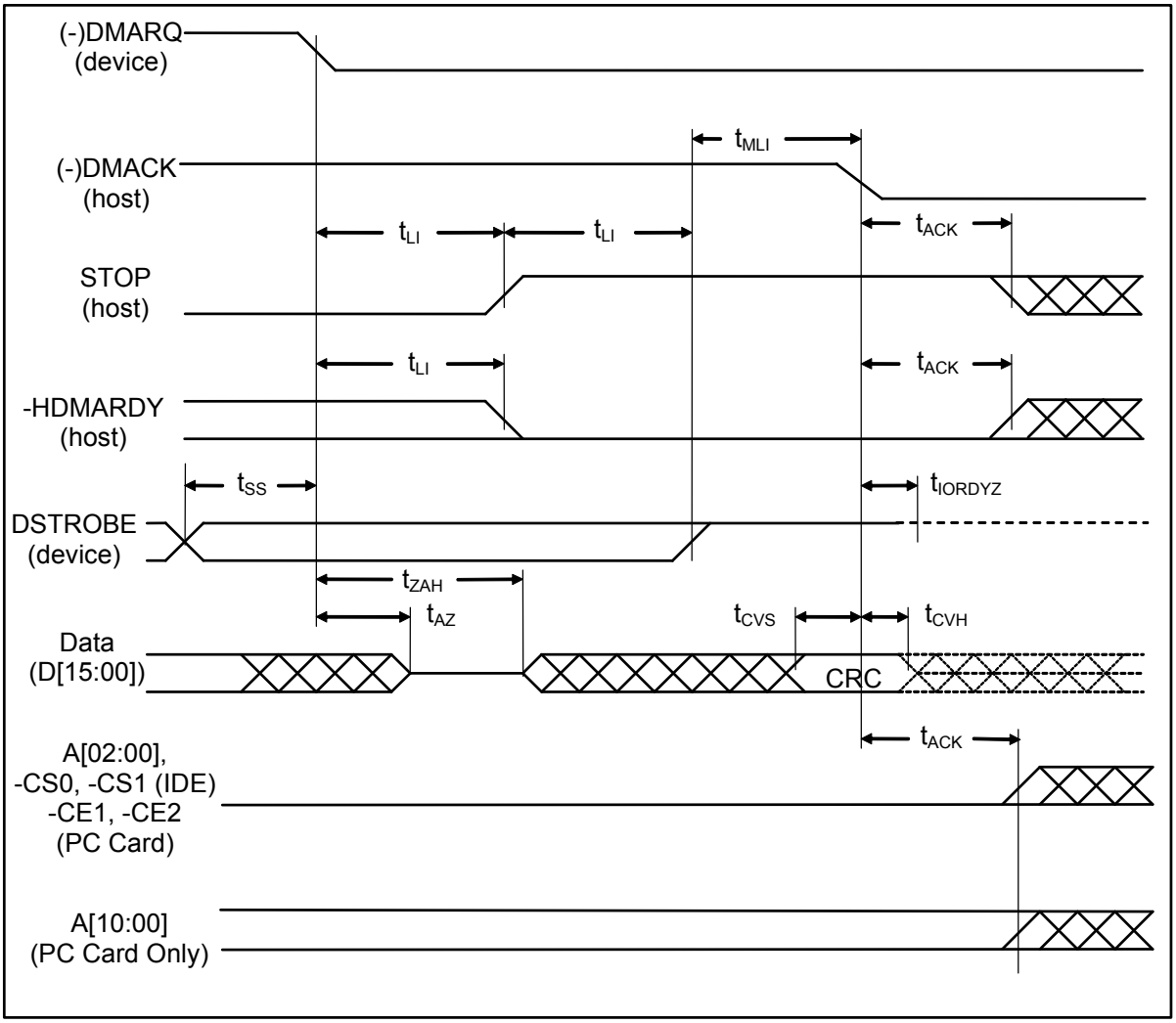
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred.

b) The device shall pause an Ultra DMA data burst by not generating DSTROBE edges.

c) NOTE – The host shall not immediately assert STOP to initiate Ultra DMA data burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate Ultra DMA data burst termination, the host shall negate -HDMARDY and wait t_{RP} before asserting STOP.

d) The device shall resume an Ultra DMA data burst by generating a DSTROBE edge.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

Figure 36: Ultra DMA Data-In Burst Device Termination Timing

4.3.18.5.5 Host Terminating an Ultra DMA Data-In Burst

The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 37: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not initiate Ultra DMA data burst termination until at least one data word of an Ultra DMA data burst has been transferred.

b) The host shall initiate Ultra DMA data burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA data burst is terminated.

c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY

d) While operating in Ultra DMA modes 2, 1, or 0 the host shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The host shall assert STOP no sooner than t_{RP} after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA data burst is terminated.

f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA data burst is terminated.

g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA data burst is terminated.

h) The device shall release D[15:00] no later than t_{AZ} after negating DMARQ.

i) The host shall drive D[15:00] no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation (see 4.3.18.6 Ultra DMA CRC Calculation).

j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00] (see 4.3.18.6 Ultra DMA CRC Calculation).

k) The host shall negate -DMACK no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than t_{DVS} after the host places the result of its CRC calculation on D[15:00].

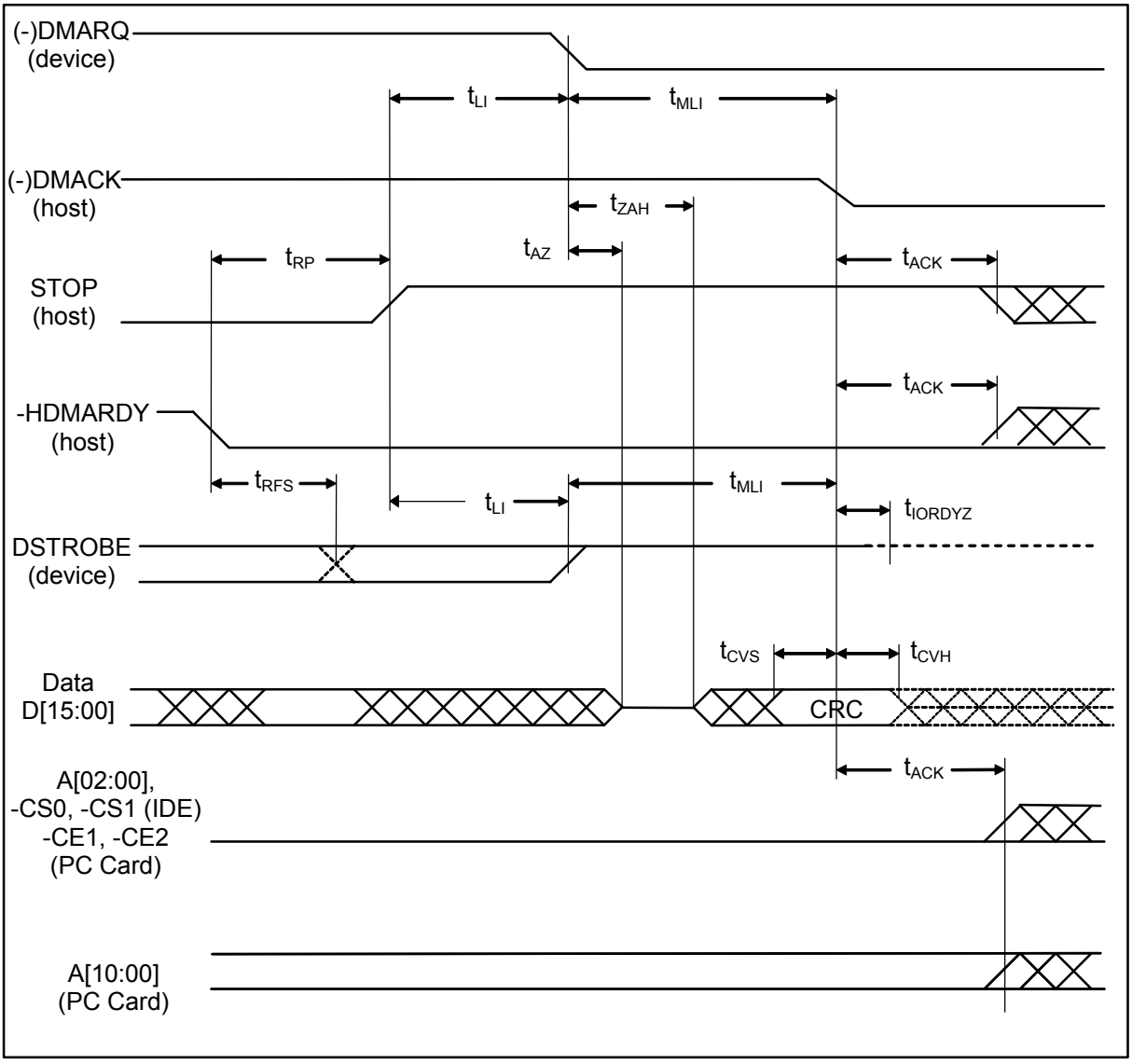
l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA data burst for any one command, at the end of the command, the device shall report the first error that occurred (see 4.3.18.6 Ultra DMA CRC Calculation)

n) While operating in True IDE mode, the device shall release DSTROBE within t_{IORDYZ} after the host negates -DMACK.

o) The host shall neither negate STOP nor assert -HDMARDY until at least t_{ACK} after the host has negated -DMACK.

p) In True IDE mode, the host shall not assert -IORD, -CS0, -CS1, nor A[02:00] until at least t_{ACK} after negating DMACK. In PC Card modes, the host shall not assert -IORD, -CE1, or -CE2, nor change A[10:00] in PC Card modes until at least t_{ACK} after negating DMACK.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 37: Ultra DMA Data-In Burst Host Termination Timing

4.3.18.5.6 Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 38: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall keep -DMACK in the negated state before an Ultra DMA data burst is initiated.

b) The device shall assert DMARQ to initiate an Ultra DMA data burst.

c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

d) The host shall assert HSTROBE.

e) In True IDE mode, the host shall not assert -CS0, -CS1, nor A[02:00]. In PC Card modes, the host shall not assert -CE1 nor -CE2 and shall hold A[10:0] fixed until after negating -DMACK at the end of the burst

f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA data burst.

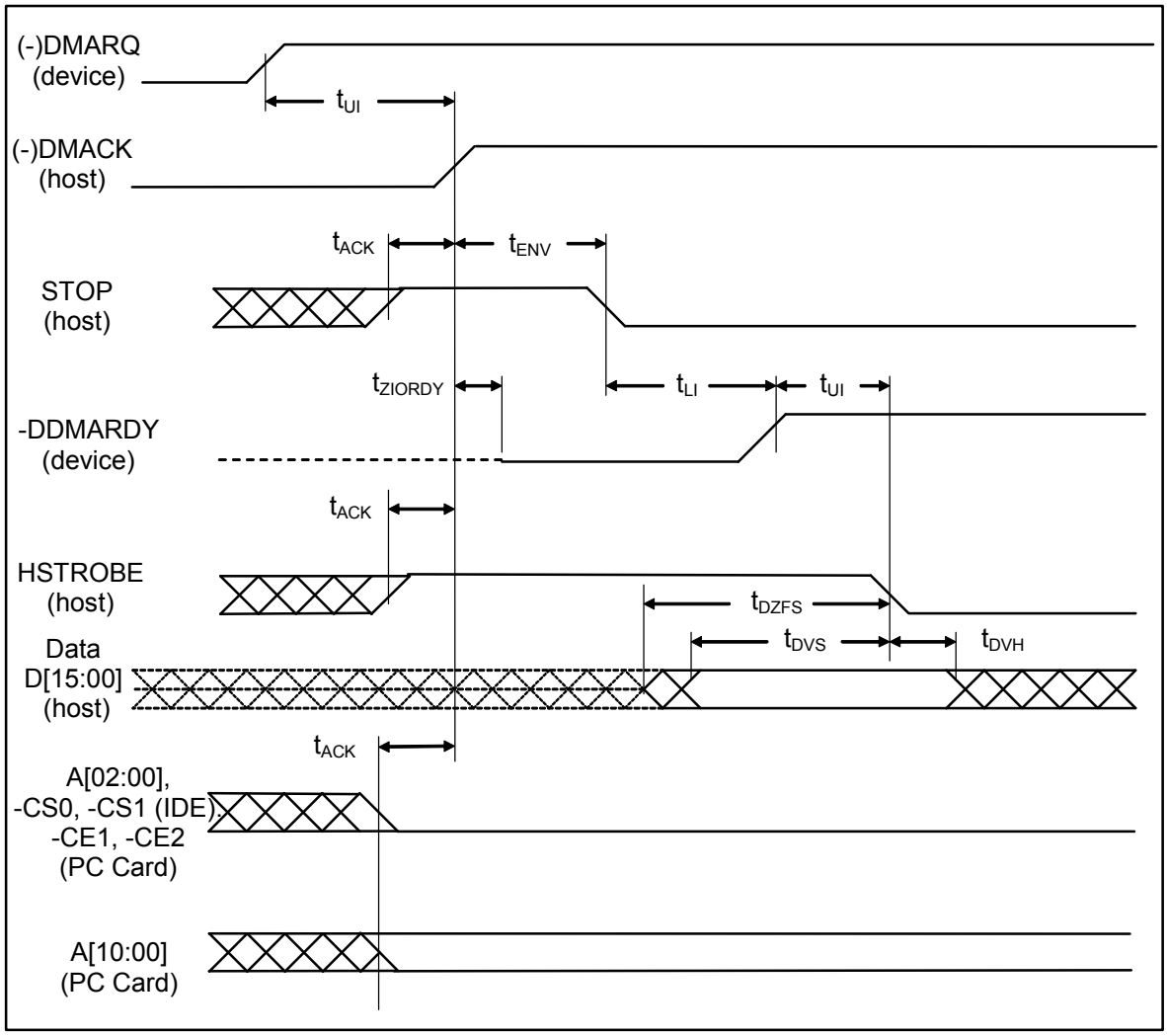
g) The device may negate -DDMARDY t_{ZIORDY} after the host has asserted -DMACK. While operating in True IDE mode, once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA data burst.

h) The host shall negate STOP within t_{ENV} after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.

i) The device shall assert -DDMARDY within t_{LI} after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.

j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA data burst initiation.

k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto D[15:00].



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 38: Ultra DMA Data-Out Burst Initiation Timing

4.3.18.5.7 Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 39: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

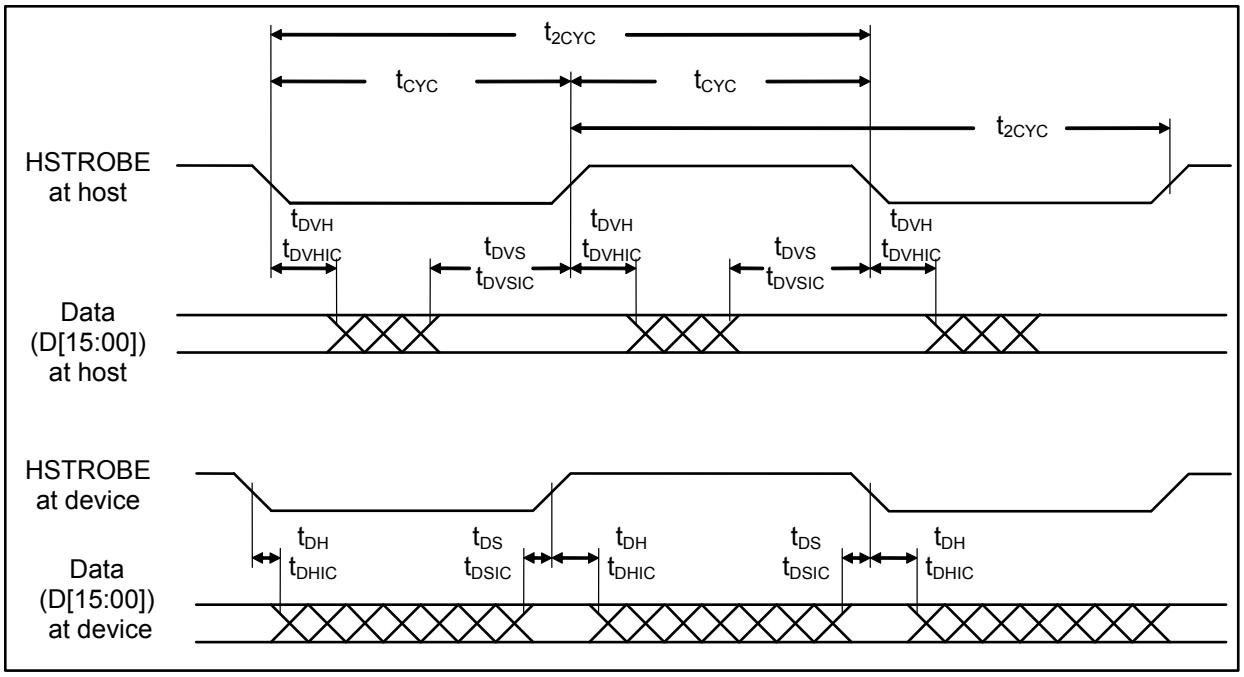
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall drive a data word onto D[15:00].

b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than $2t_{cyc}$ for the selected Ultra DMA mode.

c) The host shall not change the state of D[15:00] until at least t_{DVH} after generating an HSTROBE edge to latch the data.

d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA data burst is paused, whichever occurs first.



Note: Data (D[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

Figure 39: Sustained Ultra DMA Data-Out Burst Timing

4.3.18.5.8 Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 40: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

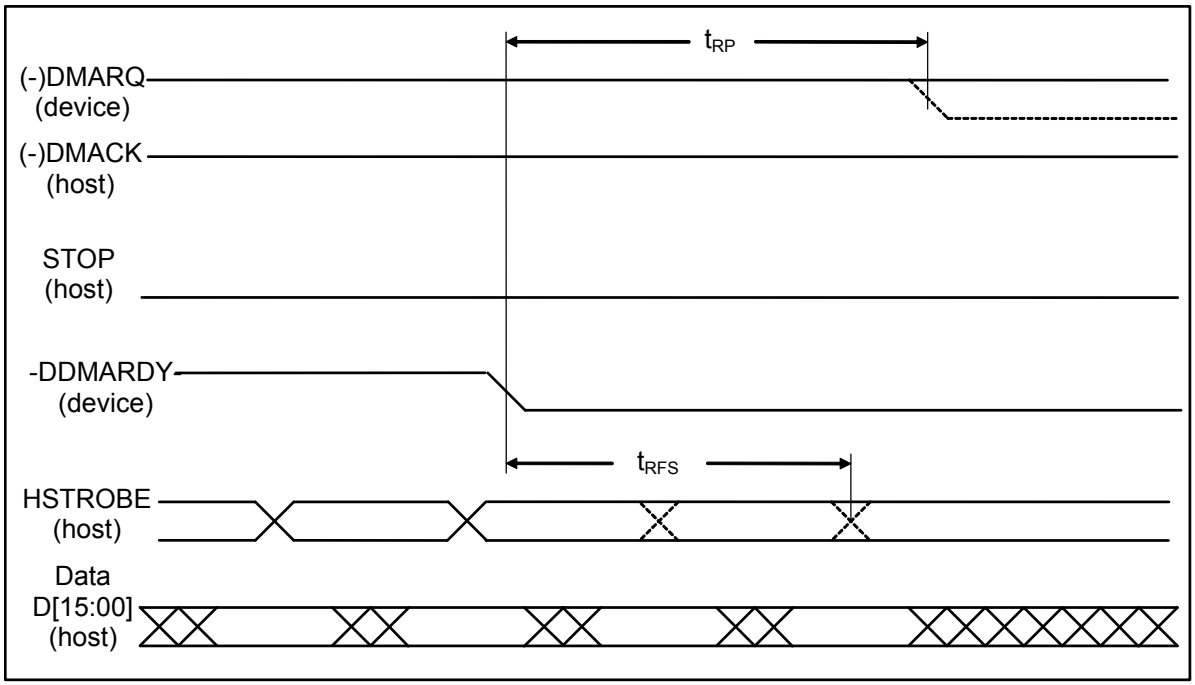
a) The device shall not pause an Ultra DMA data burst until at least one data word of an Ultra DMA data burst has been transferred.

b) The device shall pause an Ultra DMA data burst by negating -DDMARDY.

c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating -DDMARDY.

d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The device shall resume an Ultra DMA data burst by asserting -DDMARDY.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: 1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than t_{RP} after -DDMARDY is negated.

2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

3) The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 40: Ultra DMA Data-Out Burst Device Pause Timing

4.3.18.5.9 Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 41: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not initiate Ultra DMA data burst termination until at least one data word of an Ultra DMA data burst has been transferred.

b) The device shall initiate Ultra DMA data burst termination by negating -DDMARDY.

c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating -DDMARDY.

d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The device shall negate DMARQ no sooner than t_{RP} after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA data burst is terminated.

f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA data burst is terminated.

g) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA data burst is terminated.

h) The host shall place the result of its CRC calculation on D[15:00] (see 4.3.18.6 Ultra DMA CRC Calculation).

i) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].

j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA data bursts for any one command, the device shall report the first error that occurred (see 4.3.18.6 Ultra DMA CRC Calculation).

l) While operating in True IDE mode, the device shall release DSTROBE within t_{IORDYZ} after the host negates -DMACK.

m) The host shall not negate STOP nor assert –HDMARDY until at least t_{ACK} after negating -DMACK.

n) In True IDE mode, the host shall not assert -IOWR, -CS0, -CS1, nor A[02:00] until at least t_{ACK} after negating DMACK. In PC Card modes, the host shall not assert -IOWR, -CE1 nor -CE2 and shall hold A[10:00] fixed until at least t_{ACK} after negating DMACK.

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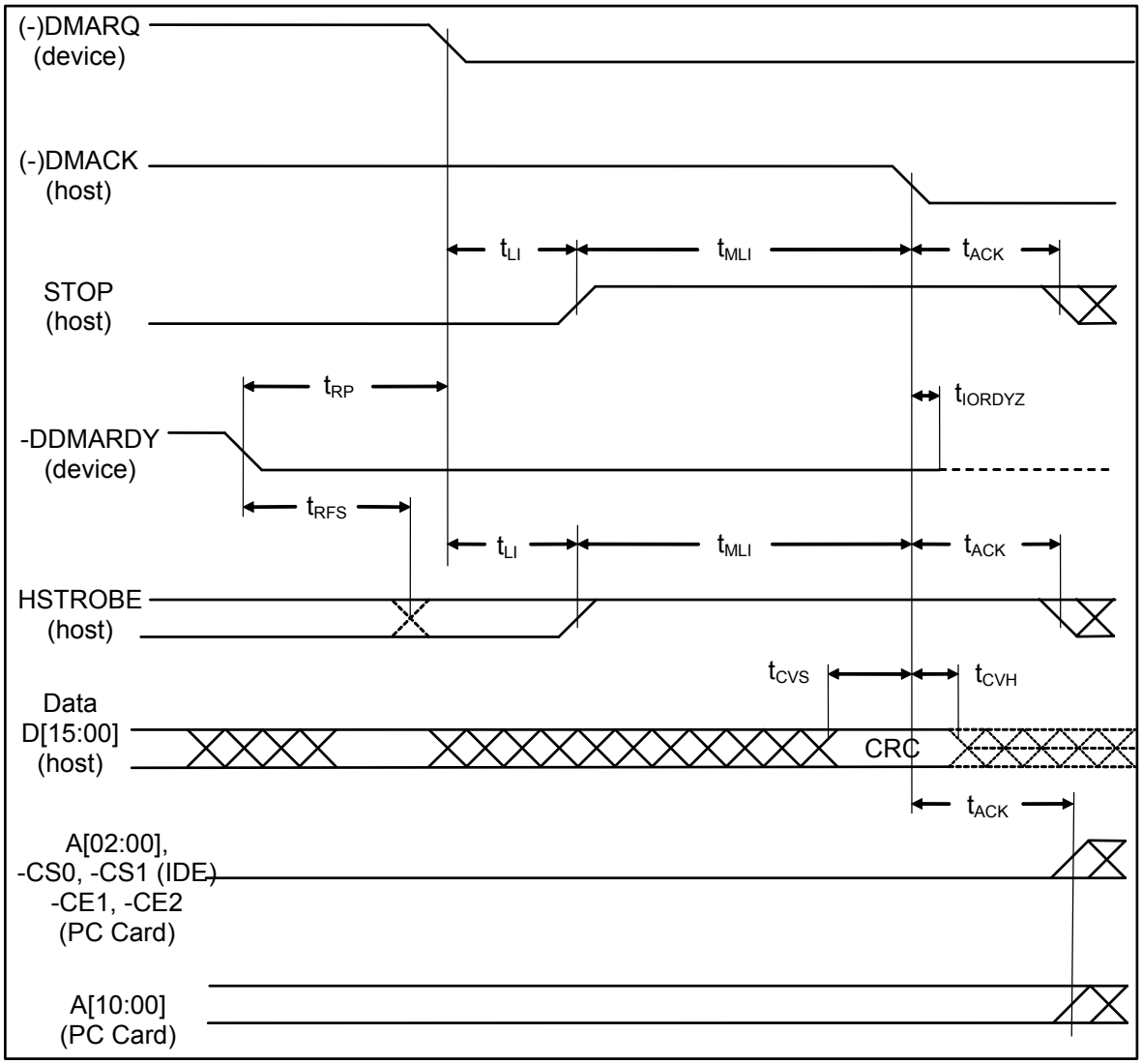


ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A00-A02, -CS0 & -CS1 are True IDE mode signal definitions. A00-A10, -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 41: Ultra DMA Data-Out Burst Device Termination Timing

4.3.18.5.10 Host Terminating an Ultra DMA Data-Out Burst

Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 42: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 25: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Table 26: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall initiate termination of an Ultra DMA data burst by not generating HSTROBE edges.

b) The host shall assert STOP no sooner than t_{SS} after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA data burst is terminated.

c) The device shall negate DMARQ within t_{LI} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA data burst is terminated.

d) The device shall negate -DDMARDY within t_{LI} after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA data burst termination is complete.

e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA data burst is terminated.

f) The host shall place the result of its CRC calculation on D[15:00] (see 4.3.18.6 Ultra DMA CRC Calculation).

g) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].

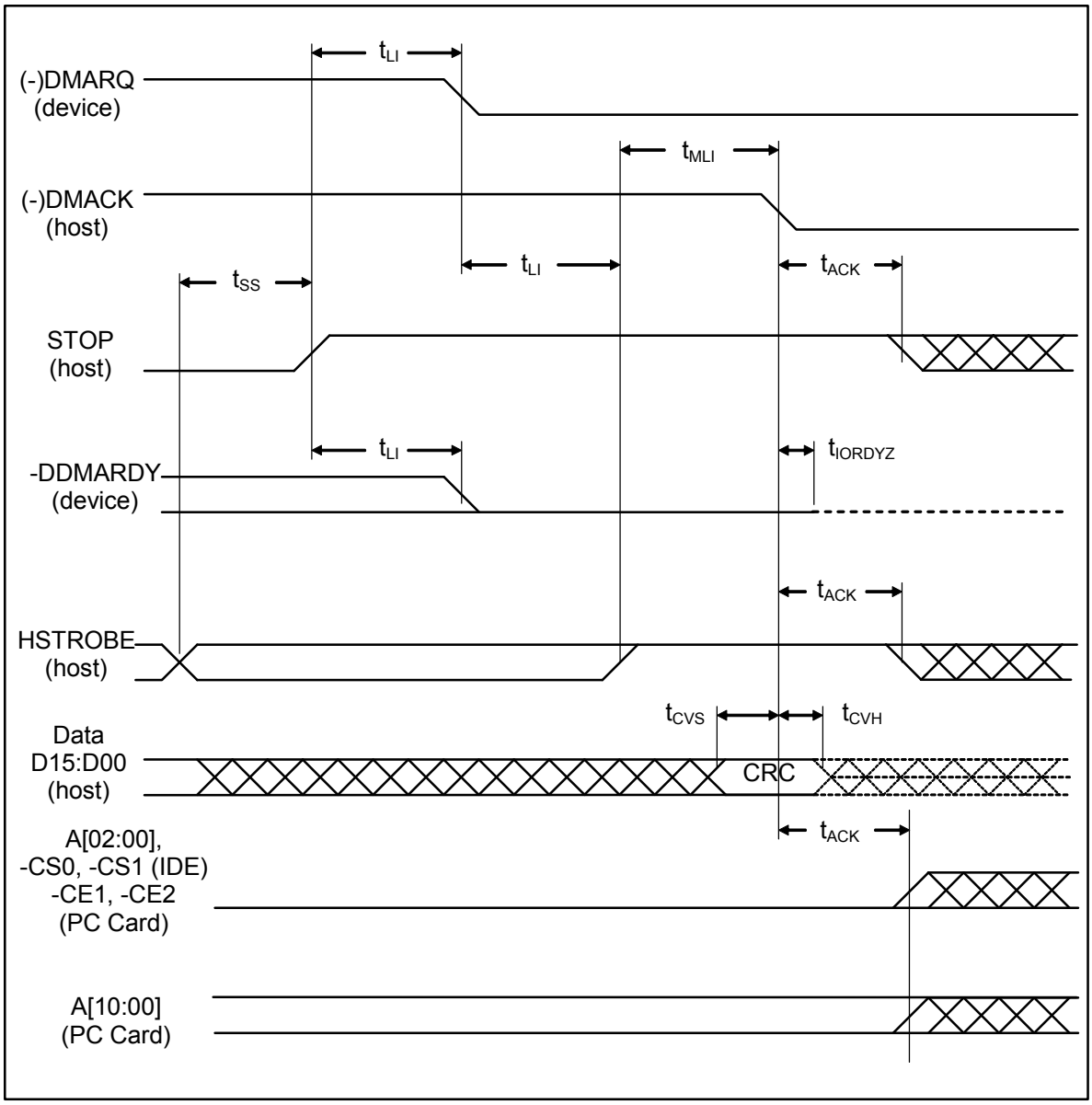
h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA data bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 4.3.18.6 Ultra DMA CRC Calculation).

j) While operating in True IDE mode, the device shall release -DDMARDY within t_{IORDYZ} after the host has negated -DMACK.

k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating -DMACK.

l) In True IDE mode, the host shall not assert -IOWR, -CS0, -CS1, nor A[02:00] until at least t_{ACK} after negating DMACK. In PC Card modes, the host shall not assert -IOWR, -CE1 nor -CE2 and shall hold A[10:00] fixed until at least t_{ACK} after negating DMACK.



ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.
NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

Figure 42: Ultra DMA Data-Out Burst Host Termination Timing

4.3.18.6 Ultra DMA CRC Calculation

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA data burst, and reporting any error that occurs at the end of a command.

1. Both the host and the device shall have a 16-bit CRC calculation function.

2. Both the host and the device shall calculate a CRC value for each Ultra DMA data burst.

3. The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA data burst before any data is transferred.

4. For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA data burst termination request has been acknowledged.

5. At the end of any Ultra DMA data burst the host shall send the results of its CRC calculation function to the device on D[15:00] with the negation of -DMACK.

6. The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA data burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA data burst in the same command. If a miscompare error occurs during one or more Ultra DMA data bursts for any one command, at the end of the command, the device shall report the first error that occurred.

7. For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands: When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the “Interface CRC Error” bit. The host shall respond to this error by re-issuing the command.

8. For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command): When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.

9. For any packet command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.

   NOTE – If excessive CRC errors are encountered while operating in Ultra mode 2 or 1, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.

10. A host may send extra data words on the last Ultra DMA data burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.

11. The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 28 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).

    NOTE – Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where D00 is shifted in first and D15 is shifted in last.

Table 29: Equations for parallel generation of an Ultra DMA CRC

CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = D00 XOR CRCOUT15	f9 = D08 XOR CRCOUT7 XOR f5
f2 = D01 XOR CRCOUT14	f10 = D09 XOR CRCOUT6 XOR f6
f3 = D02 XOR CRCOUT13	f11 = D10 XOR CRCOUT5 XOR f7
f4 = D03 XOR CRCOUT12	f12 = D11 XOR CRCOUT4 XOR f1 XOR f8
f5 = D04 XOR CRCOUT11 XOR f1	f13 = D12 XOR CRCOUT3 XOR f2 XOR f9
f6 = D05 XOR CRCOUT10 XOR f2	f14 = D13 XOR CRCOUT2 XOR f3 XOR f10
f7 = D06 XOR CRCOUT9 XOR f3	f15 = D14 XOR CRCOUT1 XOR f4 XOR f11
f8 = D07 XOR CRCOUT8 XOR f4	f16 = D15 XOR CRCOUT0 XOR f5 XOR f12

Notes: 1) f=feedback

2) D[15:0] = Data to or from the bus

3) CRCOUT = 16-bit edge triggered result (current CRC)

4) CRCOUT[15:0] are sent on matching order bits of D[15:00]

An example of a CRC generator implementation is provided below in Figure 43: Ultra DMA Parallel CRC Generator Example.

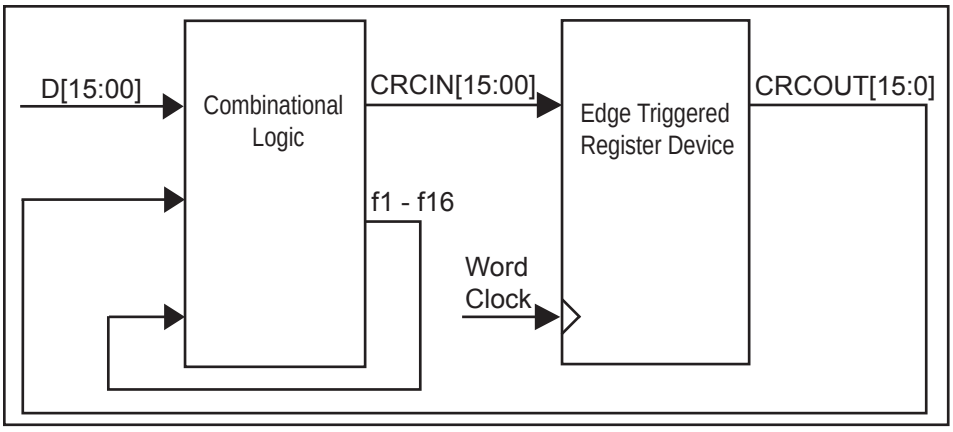


Figure 43: Ultra DMA Parallel CRC Generator Example

4.4 Card Configuration

The CompactFlash Storage Cards and CF+ Cards are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card or CF+ Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

4.4.1 Single Function CF+ Cards

Single function CF+ Cards shall have a single configuration tuple describing a single set of Function Configuration registers (see the *Metaformat Specification*). All single function CF+ Card configurations are performed using this set of Function Configuration registers.

4.4.2 Multiple Function CF+ Cards

Multiple function CF+ Cards shall have a separate set of Configuration registers for each function on the card. Multiple Function CF+ Cards shall use a combination of a global CIS common to all functions on the card and a separate function-specific CIS specific to each function on the card. The global CIS describes features that are common to all functions on the card. A CISTPL_LONGLINK_MFC tuple in the global CIS describes the location of a function-specific CIS for each function on the CF+ Card.

NOTE: a CISTPL_FUNCID with a TPLFID_FUNCTION field reset to zero (0) shall not be placed in the CIS of a Multiple Function CF+ Card. This tuple is reserved for vendor-specific multiple function CF+ Cards that do not follow the multiple function *CF+* definitions in the Standard.

Table 30: CompactFlash Storage Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby and UDMA transfer
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Table: 31 PC Card Memory Mode UDMA Function

-CE2	-CE1	-DMARQ -INPACK	-DMACK -REG	STOP -IOWR	-DMARDY -IORD (R) -WAIT (W)	STROBE -WAIT (R) -IORD (W)	DMA CMD	A10-A00	Operation
1	1	1	X	X	X	X	No	XX	Standby
X	X	0	1	X	X	1	YES	XX	Device UDMA Transfer Request (Assert DMARQ)
X	X	0	1	1	X	1	YES	XX	Host Acknowledge Preparation
1	1	0	1	1	1	1	YES	Static	Host Acknowledge Preparation
1	1	0	0	1	1	1	YES	Static	DMA Acknowledge (Stopped)
1	1	0	0	0	0	1	YES	Static	Burst Initiation / Active
1	1	0	0	0	X	/ or \	YES	Static	Burst Transfer
1	1	0	0	0	1	0 or 1	RD	Static	Data In Burst Host Pause
1	1	0	0	0	0	0 or 1	RD	Static	Data In Burst Device Pause
1	1	0	0	0	1	0 or 1	WR	Static	Data Out Burst Device Pause
1	1	0	0	0	0	0 or 1	WR	Static	Data Out Burst Host Pause
1	1	1	0	0	0	0 or 1	RD	Static	Device Initiating Burst Termination
1	1	1	0	1	1	0 or 1	RD	Static	Host Acknowledement of Device Initiated Burst Termination
1	1	0	0	1	0	0 or 1	YES	Static	Host Initiating Burst Termination
1	1	1	0	1	1	0 or 1	YES	Static	Device Acknowledging Host Initiated Burst Termination
1	1	1	0	1	1	/	YES	Static	Device Aligning STROBE to Asserted before CRC Transfer
1	1	1	/	1	1	1	YES	Static	CRC Data Transfer for UDMA Burst
1	1	1	1	1	1	1	YES	Static	Burst Completed

Table 32: CompactFlash Storage Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Table 33: CF+ Card Register and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10-A1	A0	SELECTED SPACE
1	1	X	X	X	XXX	X	Standby
X	0	0	0	1	XXX	0	Configuration Registers Read
1	0	1	0	1	XXX	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	XXX	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	XXX	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	XXX	0	Configuration Registers Write
1	0	1	1	0	XXX	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	XXX	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	XXX	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	XXX	0	Card Information Structure Read
1	0	0	1	0	XXX	0	Invalid Access (CIS Write)
1	0	0	0	1	XXX	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	XXX	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	XXX	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	XXX	X	Invalid Access (Odd Attribute Write)

Table 34: CF+ Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10 -A5	A4	A3	A2	A1	A0	Selected Register
X	0	0	0	1	XX	0	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	XX	0	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	XX	0	0	0	1	0	Card Status Register Read
X	0	0	1	0	XX	0	0	0	1	0	Card Status Register Write
X	0	0	0	1	XX	0	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	XX	0	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	XX	0	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	XX	0	0	1	1	0	Socket and Copy Register Write
X	0	0	0	1	XX	0	1	0	0	0	Reserved
X	0	0	1	0	XX	0	1	0	1	0	I/O Base 0
X	0	0	0	1	XX	0	1	1	0	0	I/O Base 1
X	0	0	1	0	XX	0	1	1	1	0	Reserved
X	0	0	0	1	XX	1	0	0	0	0	Reserved
X	0	0	1	0	XX	1	0	0	1	0	I/O Limit
X	0	0	0	1	XX	1	0	1	0	0	Reserved

Note: For CompactFlash Storage Cards, the location of the card configuration registers should always be read from the CIS since these locations may vary in future products. For CF+ Cards, the location of the card configuration registers shall always be read from the CIS. No writes should be performed to the CompactFlash Storage Card or CF+ Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

4.4.3 Attribute Memory Function

Attribute memory is a space where CompactFlash Storage Card and CF+ Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the card configuration registers is 200h. For CF+ cards, the base address of the card configuration registers is determined by the Configuration tuple (CISTPL_CONFIG).

For the Attribute Memory Read function, signals -REG and -OE shall be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 35: Attribute Memory Function below for signal states and bus validity for the Attribute Memory function.

Table 35: Attribute Memory Function

Function Mode	DMA CMD	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	Don't Care	H	H	H	X	X	X	X	X	High Z	High Z
Standby Mode	No	X	H	H	X	X	X	X	X	High Z	High Z
UDMA Operation (see section 4.3.18: Ultra DMA Mode Read/Write Timing Specification)	Yes	L[1]	H	H	X	X	X	H	H	Odd Byte	Even Byte
Read Byte Access CIS ROM (8 bits)	No	L	H	L[2]	L	L	L	L[2]	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	No	L	H	L[2]	L	L	L	H	L[2]	Don't Care	Even Byte
Read Byte Access Configuration CompactFlash Storage (8 bits)	No	L	H	L	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration CompactFlash Storage (8 bits)	No	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration *CF+* (8 bits)	No	L	H	L	X	X	L	L	H	High Z	Even Byte
Write Byte Access Configuration *CF+* (8 bits)	No	L	H	L	X	X	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	No	L	L[2]	L[2]	L	L	X	L[2]	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	No	L	L[2]	L[2]	L	L	X	H	L[2]	Don't Care	Even Byte
Read Word Access Configuration CompactFlash Storage (16 bits)	No	L	L[2]	L[2]	L	H	X	L[2]	H	Not Valid	Even Byte
Write Word Access Configuration CompactFlash Storage (16 bits)	No	L	L[2]	L[2]	L	H	X	H	L[2]	Don't Care	Even Byte
Read Word Access Configuration *CF+* (16 bits)	No	L	L[2]	L[2]	X	X	X	L[2]	H	Not Valid	Even Byte
Write Word Access Configuration *CF+* (16 bits)	No	L	L[2]	L[2]	X	X	X	H	L[2]	Don't Care	Even Byte

Notes: 1) In UDMA operation, the -REG (-DMACK) signal shall be asserted only in response to -DMARQ.

2) The -CE signals or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.

4.4.4 Configuration Option Register (Base + 00h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Storage Card or CF+ Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Figure 44: Configuration Option Register

SRESET - Soft Reset: setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash Storage Card or CF+ Card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash Storage Card or CF+ Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. For CompactFlash Storage Cards, using the PCMCIA PC Card Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ: this bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5 - Conf0 - Configuration Index: set to zero (0) by reset. It is used to select operation mode of the CompactFlash Storage Card or CF+ Card as shown below.

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and shall be written as zero (0). These bits are vendor defined for CF+ Cards.

Table 36: CompactFlash Storage Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0h-1F7h/3F6h-3F7h
0	0	0	0	1	1	I/O Mapped, 170h-177h/376h-377h

Table 37: CF+ Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	CF+ Card Mode
0	0	0	0	0	0	Memory Mapped, I/O cycles are ignored
X	X	X	X	X	X	Any non-zero value, vendor defined

On Multiple Function CF+ Cards, bits in this field enable the following functionality:

Conf0	**Enable Function** - If this bit is reset to zero (0), the function is disabled. If this bit is set to one (1), the function is enabled.
Conf1	**Enable Base and Limit Registers** – If this bit is reset to zero (0) and Bit 0 is set to one (1), all I/O addresses on the host system are passed to the function. If this bit is set to one (1) and Bit 0 is set to one (1), then only I/O addresses that are qualified by the Base and Limit registers are passed to the function. If Bit 0 is reset to zero (0), this bit is undefined.
Conf2	**Enable -IREQ Routing** – If this bit is reset to zero (0) and Bit 0 is set to one (1), this function shall not generate interrupt requests on the CF+ Card's **-**IREQ line. If this is set to one (1) and Bit 0 is set to one (1), this function shall generate interrupt requests on the CF+ Card's **-**IREQ line. If Bit 0 is reset to zero (0), this bit is undefined.
Conf[5:3]	Reserved for vendor implementation.

4.4.5 Card Configuration and Status Register (Base + 02h in Attribute Memory)

The Card Configuration and Status Register contains information about the Card's condition.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	-XE	Audio	PwrDwn	Int	0
Write	0	SigChg	IOis8	-XE	Audio	PwrDwn	0	0

Figure 45: Card Configuration and Status Register

Changed: indicates that one or both of the Pin Replacement register CReady, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the CompactFlash Storage Card or CF+ Card is configured for the I/O interface.

SigChg: this bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit controls pin 46, the Changed Status signal. If no state change signal is desired, this bit is set to zero (0) and pin 46 (-STSCHG) signal is then held high while the CompactFlash Storage Card or CF+ Card is configured for I/O.

IOis8: the host sets this bit to a one (1) if the CompactFlash Storage Card or CF+ Card is to be configured in an 8 bit I/O Mode. The CompactFlash Storage Card is always configured for both 8 and 16 bit I/O, so this bit is ignored. Some CF+ cards can be configured for either 8 bit I/O mode or 16 bit I/O mode, so CF+ cards may respond to this bit.

-XE: this bit is set and reset by the host to disable and enable Power Level 1 commands in CF+ cards. If the value is 0, Power Level 1 commands are enabled; if it is 1, Power Level 1 commands are disabled. Default value at power on or after reset is 0. The host may read the value of this bit to determine whether Power Level 1 commands are currently enabled. For CompactFlash cards that do not support Power Level 1, this bit has value 0 and is not writeable.

Audio: this bit is set and reset by the host to enable and disable audio information on -SPKR when the CF+ card is configured. This bit should always be zero for CompactFlash Storage cards.

PwrDwn: this bit indicates whether the host requests the CompactFlash Storage Card or CF+ Card to be in the power saving or active mode. When the bit is one (1), the CompactFlash Storage Card or CF+ Card enters a power down mode. When PwrDwn is zero (0), the host is requesting the CompactFlash Storage Card or CF+ Card to enter the active mode. The PCMCIA PC Card READY value becomes false (busy) when this bit is changed. READY shall not become true (ready) until the power state requested has been entered. The CompactFlash Storage Card automatically powers down when it is idle and powers back up when it receives a command.

Int: this bit represents the internal state of the interrupt request. This value is available whether or not the I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

4.4.6 Pin Replacement Register (Base + 04h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CReady	CWProt	1	1	RReady	WProt
Write	0	0	CReady	CWProt	0	0	MReady	MWProt

Figure 46: Pin Replacement Register

CReady: this bit is set to one (1) when the bit RReady changes state. This bit can also be written by the host.

CWProt: this bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RReady: this bit is used to determine the internal state of the READY signal. This bit may be used to determine the state of the READY signal as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask (MReady) for writing the corresponding bit CReady.

WProt: this bit is always zero (0) since the CompactFlash Storage Card or CF+ Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MReady: this bit acts as a mask for writing the corresponding bit CReady.

MWProt: this bit when written acts as a mask for writing the corresponding bit CWProt.

Table 38: Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final	Comments
	"C" Bit	"M" Bit	"C" Bit	
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

4.4.7 Socket and Copy Register (Base + 06h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is not required for CF or CF+ Cards.

If present, it is optional for a CF Card to allow setting bit D4 (Drive number) to 1. If two drives are supported, it is intended for use only when two cards are co-located at either the primary or secondary addresses in PC Card I/O mode. The availability and capabilities of this register are described in the Card Information Structure of the CF Card.

Hosts shall not depend on the availability of this functionality.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Obsolete[1] (Drive #)	0	0	0	0
Write	0	0	0	Obsolete[1] (Drive #)	X	X	X	X

Figure 47: Socket and Copy Register

Reserved: this bit is reserved for future standardization. This bit shall be set to zero (0) by the software when the register is written.

Obsolete (Drive #): this bit is obsolete and should be written as 0.

If the obsolete functionality is not supported it shall be read as written or shall be read as 0. If the obsolete functionality is supported, the bit shall be read as written. If supported, this bit sets the drive number, which the card matches with the DRV bit of the Drive/Head register when configured in a twin card configuration.

It is recommended that the host always write 0 for the drive number in this register and in the DRV bit of the Drive/Head register for PC Card modes of operation.

X: the socket number is ignored by the CompactFlash Storage Card.

4.4.8 I/O Base Register (0, 1)

The I/O Base registers are optional on single function CF+ Cards and are required on multiple function CF+ Cards. The I/O Base registers determine the base address of the I/O range used to access function-specific registers on the CF+ Card. These registers allow the CF+ Card's function-specific registers to be placed anywhere in the host system's I/O address space. The registers are written in little-endian order with the least significant byte of the base I/O address written to I/O Base 0.

The number of I/O Base Address registers implemented depends on the number of address lines the CF+ Card decodes. For example, if the function on the CF+ Card only decodes eight (8) address lines, only the first register needs to be implemented.

Offset	D7	D6	D5	D4	D3	D2	D1	D0
10	I/O Base 0							
12	I/O Base 1							

Figure 48: I/O Base Registers (0, 1)

4.4.9 I/O Limit Register

The I/O Limit register is an optional register and is only implemented on CF+ Cards that use I/O Base Address registers. If the function on the CF+ Card always uses the same number of I/O registers in all configurations, this register may be omitted (even on CF+ Cards with I/O Base Address registers).

This register specifies the number of address lines used by the function. Each bit in the register represents an I/O address line. This allows two (2) to two hundred and fifty-six (256) I/O ports to be used by a function. If a bit in the register is set to one (1), all bits of lesser significance in the register shall also be set to one (1).

Offset	D7	D6	D5	D4	D3	D2	D1	D0
18	I/O Limit							

Field	Type	Description
I/O Limit	R/W	Bit-mapped register indicating the number of I/O address lines decoded by the function on the CF+ Card.

Figure 49: I/O Limit Register

4.5 I/O Transfer Function

4.5.1 I/O Function

The I/O transfer to or from the CompactFlash Storage or CF+ Card can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage or CF+ Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage or CF+ Card, the system shall generate a pair of 8 bit references to access the word's even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds. CF+ cards may or may not allow 16 bit register accesses and thus shall assert -IOIS16 as required.

The CompactFlash Storage and CF+ Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 39: PC Card Mode I/O Function

Function Code	DMA CMD	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	No	X	H	H	X	X	X	High Z	High Z
UDMA Write	Write	H	H	H	X	X	X	Odd Byte	Even Byte
UDMA Read	Read	H	H	H	X	X	X	Odd Byte	Even Byte
Byte Input Access (8 bits)	X	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	X	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	X	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	X	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	X	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	X	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	X	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	X	L	L	H	X	H	L	Odd-Byte	Don't Care

Table: 40 PC Card I/O Mode UDMA Function

-CE2	-CE1	-DMARQ -INPACK	DMACK -REG	STOP -IOWR	-DMARDY -IORD (R) -WAIT (W)	STROBE -WAIT (R) -IORD (W)	DMA CMD	A10-A00	Operation
1	1	1	X	X	X	X	No	XX	Standby
X	X	0	0	X	X	1	YES	XX	Device UDMA Transfer Request (Assert DMARQ)
X	X	0	0	1	X	1	YES	XX	Host Acknowledge Preparation
1	1	0	0	1	1	1	YES	Static	Host Acknowledge Preparation
1	1	0	1	1	1	1	YES	Static	DMA Acknowledge (Stopped)
1	1	0	1	0	0	1	YES	Static	Burst Initiation / Active
1	1	0	1	0	X	/ or \	YES	Static	Burst Transfer
1	1	0	1	0	1	0 or 1	RD	Static	Data In Burst Host Pause
1	1	0	1	0	0	0 or 1	RD	Static	Data In Burst Device Pause
1	1	0	1	0	1	0 or 1	WR	Static	Data Out Burst Device Pause
1	1	0	1	0	0	0 or 1	WR	Static	Data Out Burst Host Pause
1	1	1	1	0	0	0 or 1	RD	Static	Device Initiating Burst Termination
1	1	1	1	1	1	0 or 1	RD	Static	Host Acknowledement of Device Initiated Burst Termination
1	1	0	1	1	0	0 or 1	YES	Static	Host Initiating Burst Termination
1	1	1	1	1	1	0 or 1	YES	Static	Device Acknowledging Host Initiated Burst Termination
1	1	1	1	1	1	/	YES	Static	Device Aligning STROBE to Asserted before CRC Transfer
1	1	1	\	1	1	1	YES	Static	CRC Data Transfer for UDMA Burst
1	1	1	0	1	1	1	YES	Static	Burst Completed

4.6 Common Memory Transfer Function

4.6.1 Common Memory Function

The Common Memory transfer to or from the CompactFlash Storage or CF+ Card can be either 8 or 16 bits.

The CompactFlash Storage Card and the CF+ Card permit both 8 and 16 bit accesses to all of its Common Memory addresses.

The CompactFlash Storage Card or the CF+ Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 41: Common Memory Function

Function Code	DMA	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	None	X	H	H	X	X	X	High Z	High Z
Byte Read (8 bits)	Don't Care	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write (8 bits)	Don't Care	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read (16 bits)	Don't Care	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write (16 bits)	Don't Care	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	Don't Care	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	Don't Care	H	L	H	X	H	L	Odd-Byte	Don't Care
Ultra DMA Write	Write	L	H	H	X	H	H	Odd-Byte	Even-Byte
Ultra DMA Read	Read	L	H	H	X	H	H	Odd-Byte	Even-Byte

4.7 True IDE Mode I/O Transfer Function

4.7.1 True IDE Mode I/O Function

The CompactFlash Storage Card and CF+ Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash Storage Cards and CF+ Cards may support the following optional detection methods:

1. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to PC Card mode upon detecting a high level on the pin.

2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin.

3. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time.

Host implementers should not rely on any of these optional detection methods in their designs. In the True IDE Mode, the PCMCIA PC Card protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. CompactFlash Storage Cards permit 8 bit PIO mode data accesses if the user issues a Set Feature Command to put the CompactFlash Storage Card in 8 bit Mode.

Note: Removing and reinserting the CompactFlash Storage Card while the host computer's power is on will reconfigure the CompactFlash Storage Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Storage Card in True IDE Mode, the 50-pin socket is power cycled with the CompactFlash Storage Card inserted and -OE (output enable) asserted.

CF+ Card support of True IDE mode is optional.

Table 42: True IDE Mode I/O Function defines the function of the operations for the True IDE Mode.

Table 42: True IDE Mode I/O Function

Function Code	-CS1	-CS0	A0-A2	DMARQ	-DMACK	-IORD	-IOWR	D15-D8	D7-D0
Invalid Modes	L	L	X	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	X	L	X	L	Undefined In	Undefined In
	X	X	X	L	L	X	X	Undefined In/Out	Undefined In/Out
Standby Mode	H	H	X	L	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	L	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	L	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	H	L	H	L	Odd-Byte In	Even-Byte In
Ultra DMA Data Register Write	H	H	0	H	L	See Note 2		Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	L	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	H	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	0	H	L	See Note 3		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	L	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	L	H	L	H	High Z	Status Out
Drive Address[1]	L	H	7h	L	H	L	H	High Z	Data Out

Notes: 1) Implemented for backward compatibility. Bit D7 of the register shall remain High Z to prevent conflict with any floppy disk controller at the same address. The host software should not rely on the contents of this register.

2) In Ultra DMA Data Register Write mode the signals –IORD, –IOWR and IORDY are redefined and used as follows: –IORD as HSTROBE, –IOWR as STOP and IORDY as –DDMARDY. Data transfers with each edge of HSTROBE. See Section 4.3.18: Ultra DMA Mode Read/Write Timing Specification and Table 5: Signal Description for complete information.

3) In Ultra DMA Data Register Read mode the signals –IORD, –IOWR and IORDY are redefined and used as follows: –IORD as –HDMARDY H, –IOWR as STOP and IORDY as DSTROBE. Data transfers with each edge of DSTROBE. See Section 4.3.18: Ultra DMA Mode Read/Write Timing Specification and Table 5: Signal Description for complete information.

4.8 Host Configuration Requirements for Master/Slave or New Timing Modes

The CF Advanced Timing modes include PCMCIA PC Card style I/O modes that are faster than the original 250 ns cycle time. These modes are not supported by the PCMCIA PC Card specification nor CF by cards based on revisions of the CF specification before Revision 3.0. Hosts shall ensure that all cards accessed through a common electrical interface are capable of operation at the desired, faster than 250 ns, I/O mode before configuring the interface for that I/O mode.

Advanced Timing modes are PCMCIA PC Card style I/O modes that are 100 ns or faster, PC Card Memory modes that are 100ns or faster, True IDE PIO Modes 5,6 and Multiword DMA Modes 3,4. These modes are permitted to be used only when a single card is present and the host and card are connected directly, without a cable exceeding 0.15m in length. Consequently, the host shall not configure a card into an Advanced Timing Mode if two cards are sharing I/O lines, as in Master/Slave operation, nor if it is constructed such that a cable exceeding 0.15 meters is required to connect the host to the card.

The load presented to the Host by cards supporting Ultra DMA is more controlled than that presented by other CompactFlash cards. Therefore, the use of a card that does not support Ultra DMA in a Master/Slave arrangement with a Ultra DMA card can affect the critical timing of the Ultra DMA transfers. The host shall not configure a card into Ultra DMA mode when a card not supporting Ultra DMA is also present on the same interface

When the use of two cards on an interface is otherwise permitted, the host may use any mode that is supported by both cards, but to achieve maximum performance it should use its highest performance mode that is also supported by both cards.

5 Metaformat

5.1 Metaformat Overview

The goal of the Metaformat is to describe the requirements and capabilities of the CompactFlash Storage Card and CF+ Card as thoroughly as possible. This includes describing the power requirements, IO requirements, memory requirements, manufacturer information and details about the services provided.

The Metaformat is a hierarchy of layers. Each layer is numbered with a number that increases as the level of abstraction gets higher. Included are layers to describe the data recording format and data organization, for memory and ATA cards that wish to adhere to the CFA/PCMCIA specification. Below the Metaformat is the physical layer, the electrical and physical characteristics of CF+ Cards. The CF+ Metaformat conforms directly to the PCMCIA Metaformat Specification. Refer to that document for a detailed description of the Metaformat.

5.2 Metaformat Requirements

The CF+ Cards have the following Card Information Structure (CIS) requirements:

- All CF+ Cards have a CIS that describes the functionality and characteristics of the card
- The CIS of a CF+ Card shall be readable whenever the card is powered, the card is asserting READY and the card has been reset by the host after power-up in accordance with the CompactFlash Standard. This includes after the CF+ Card is configured and when the PwrDwn bit is set in the Card Configuration and Status Register. (See the *Electrical Specification*, section 4.)
- All CF+ Cards shall provide at least the mandatory Tuples as described in the PCMCIA PC Card Metaformat Specification, Tuple Summary Table.
- All linear memory CF+ Cards shall describe how they are partitioned, even if the entire CF+ Card is used as a single partition.

5.2.1 Metaformat Representation for Extended Speed Modes

The PCMCIA PC Card Device Info Tuple is used to express operating speed of Compact Flash memory mapped registers. The cycle times defined in this specification are: 250, 120, 100 and 80 nanoseconds. These cycle times can be expressed as described in Table 43 below. See the PCMCIA PC Card Metaformat, Guidelines and PC Card-ATA specifications for further information on the methods of expressing speed and other information about the capabilities of the card.

Legend for Table 43: Sample Device Info Tuple Information for Extended Speeds

Speed	Attribute Memory Relative Offset	Code	D7	D6	D5	D4	D3	D2	D1	D0	Notes
Legend	Offset N+0		Device Type				WPS	Speed Code (7=Extended)			Always Present
	Offset N+2		Extend	Extended Speed Mantissa				Extended Speed Exponent			Present if Speed Code = 7

Table 43: Sample Device Info Tuple Information for Extended Speeds

Speed	Attribute Memory Relative Offset	Code	D7	D6	D5	D4	D3	D2	D1	D0	Notes
250	N+0	D9h	Dh = Function Specific				1	1h = 250 nsec			PCMCIA Std
120	N+0	DFh	Dh = Function Specific				1	7h = Extended			CFA Defined
	N+2	12h	0	2h = 1.2				2h = * 100 nsec			
100	N+0	DCh	Dh = Function Specific				1	4h = 100 nsec			PCMCIA
80	N+0	DFh	Dh = Function Specific				1	7h = Extended			CFA Defined
	N+2	79h	0	Fh = 8.0				1h = * 10 nsec			

Note: The value “1” defined for D3 of the N+0 words indicates that no write-protect switch controls writing the ATA registers. The value “0” defined for D7 in the N+2 words indicates that there is not more than a single speed extension byte.

Alert!

The parameter values for the cycle times in the tuples above do not have detailed timings defined by PCMCIA for other than 100 and 250 nsec. Therefore, there may be ambiguity on the part of a PCMCIA PC Card host system in applying the alternate values correctly.

At present, there is no standard method of describing Extended Speed I/O timings in the Card Information Structure.

6 Software Interface

6.1 CF-ATA Drive Register Set Definition and Protocol

The CompactFlash Storage Card can be configured as a high performance I/O device through:

a) The standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary) or 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).

b) Any system decoded 16 byte I/O block using any available IRQ.

c) Memory space.

The communication to or from the CompactFlash Storage Card is done using the Task File registers, which provide all the necessary registers for control and status information related to the storage medium. The PCMCIA PC Card interface connects peripherals to the host using four register mapping methods. Table 44 is a detailed description of these methods:

Table 44: I/O Configurations

Standard Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	XX0h-XXFh	I/O Mapped 16 Contiguous Registers
2	I/O	1F0h-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170h-177h, 376h-377h	Secondary I/O Mapped

Note: Twin Card implementation is obsolete. Refer to Section 4.4.7: Socket and Copy Register (Base + 06h in Attribute Memory)for Twin Card implementation.

6.1.1 I/O Primary and Secondary Address Configurations

Table 45: Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)h	0	0	0	1	Error Register	Features	1, 2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alt Status	Device Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Note: 1) Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers, which lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2) A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

6.1.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash Storage Card, the registers are accessed in the block of I/O space decoded by the system as follows:

Table 46: Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card /Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Notes: 1) Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2) Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.

Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data shall be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 shall access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 shall access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 shall access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3) Address lines that are not indicated are ignored by the CompactFlash Storage Card for accessing all the registers in this table.

6.1.3 Memory Mapped Addressing

When the CompactFlash Storage Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows:

Table 47: Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1, 2
1	0	X	0	0	0	1	1	Error	Features	1, 2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card /Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

Notes: 1) Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2) Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.

Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data shall be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 shall access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 shall access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 shall access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3) Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 Kbyte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.

Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA PC Card socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the CompactFlash Storage Card.

A word access to address at offset 8 shall provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the data bus.

6.1.4 True IDE Mode Addressing

When the CompactFlash Storage Card or CF+ Card is configured in the True IDE Mode, the I/O decoding is as follows:

Table 48: True IDE Mode I/O Decoding

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit[1]
1	1	X	X	X	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	0	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

Note: 1) See the section 6.1.5 CF-ATA Registers for information regarding the control of 8 or 16 bit transfers to the data register.

6.1.5 CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file."

Note: In accordance with the PCMCIA PC Card specification: each of the registers below that is located at an odd offset address may be accessed in the PC Card Memory or PC Card I/O modes at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted by the card) and an I/O cycle is being performed.

In the True IDE mode of operation, the size of the transfer is based solely on the register being addressed. All registers are 8 bit only except for the Data Register, which is normally 16 bits, but can be programmed to use 8 bit transfers for Non-DMA operations through the use of the Set Features command. The data register is also 8 bits during a portion of the Read Long and Write Long commands, which exist solely for historical reasons and should not be used.

6.1.5.1 Data Register (Address - 1F0h[170h];Offset 0,8,9)

The Data Register is a 16 bit register, and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register. Table 49: Data Register Access below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA PC Card word and byte access modes and operations. See the PCMCIA PC Card Standard, for further definitions of the Card Accessing Modes for I/O and Memory cycles.

Note: Because of the overlapped registers, PC Card modes access to the 1F1h, 171h or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. These accesses are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Table 49: Data Register Access

Data Register Memory and I/O Modes	**-CE2**	**-CE1**	**A0**	**-REG**	**Offset**	**Data Bus**
Word Data Register	0	0	X	- [1]	0,8,9	D15-D0
Even Data Register	1	0	0	- [1]	0,8	D7-D0
Odd Data Register	1	0	1	- [1]	9	D7-D0
Odd Data Register	0	1	X	- [1]	8,9	D15-D8
Error / Feature Register	1	0	1	- [1]	1, Dh	D7-D0
Error / Feature Register	0	1	X	- [1]	1	D15-D8
Error / Feature Register	0	0	X	- [1]	Dh	D15-D8
Data Register True IDE Mode	**-CS1**	**-CS0**	**A0**	**-DMACK**	**Offset**	**Data Bus**
PIO Word Data Register	1	0	0	1	0	D15-D0
DMA Word Data Register	1	1	X	0	X	D15-D0
PIO Byte Data Register (Selected Using Set Features Command)	1	0	0	1	0	D7-D0

Notes: 1) -REG signal is mode dependent. Signal shall be 0 for I/O mode and 1 for Memory Mode.

Error Register (Address - 1F1h[171h]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK/ICRC	UNC	0	IDNF	0	ABRT	0	AMNF

Figure 50: Error Register

This register is also accessed in PC Card Modes on data bits D15-D8 during a read operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK/ICRC): this bit is set when a Bad Block is detected. This bit is also set when an interface CRC error is detected in True IDE Ultra DMA modes of operation.

Bit 6 (UNC): this bit is set when an Uncorrectable Error is encountered.

Bit 5: this bit is 0.

Bit 4 (IDNF): the requested sector ID is in error or cannot be found.

Bit 3: this bit is 0.

Bit 2 (Abort) This bit is set if the command has been aborted because of a CompactFlash Storage Card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

Bit 1 This bit is 0.

Bit 0 (AMNF) This bit is set in case of a general error.

6.1.5.2 Feature Register (Address - 1F1h[171h]; Offset 1, 0Dh Write Only)

This register provides information regarding features of the CompactFlash Storage Card that the host can utilize. This register is also accessed in PC Card modes on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high.

6.1.5.3 Sector Count Register (Address - 1F2h[172h]; Offset 2)

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

6.1.5.4 Sector Number (LBA 7-0) Register (Address - 1F3h[173h]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Storage Card data access for the subsequent command.

6.1.5.5 Cylinder Low (LBA 15-8) Register (Address - 1F4h[174h]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

6.1.5.6 Cylinder High (LBA 23-16) Register (Address - 1F5h[175h]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

6.1.5.7 Drive/Head (LBA 27-24) Register (Address 1F6h[176h]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Figure 51: Drive/Head Register

Bit 7: this bit is specified as 1 for backward compatibility reasons. It is intended that this bit will become obsolete in a future revision of the specification. This bit is ignored by some controllers in some commands.

Bit 6: LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

LBA7-LBA0: Sector Number Register D7-D0.

LBA15-LBA8: Cylinder Low Register D7-D0.

LBA23-LBA16: Cylinder High Register D7-D0.

LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5: this bit is specified as 1 for backward compatibility reasons. It is intended that this bit will become obsolete in a future revisions of the specification. This bit is ignored by some controllers in some commands.

Bit 4 (DRV): DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. Setting this bit to 1 is obsolete in PCMCIA PC Card modes of operation. If the obsolete functionality is support by a CF Storage Card, the CompactFlash Storage Card is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA PC Card Socket & Copy configuration register.

Bit 3 (HS3): when operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2): when operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1): when operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0): when operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

6.1.5.8 Status & Alternate Status Registers (Address 1F7h[177h]&3F6h[376h]; Offsets 7 & Eh)

These registers return the CompactFlash Storage Card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Figure 52: Status & Alternate Status Register

Bit 7 (BUSY): the busy bit is set when the CompactFlash Storage Card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

During the data transfer of DMA commands, the Card shall not assert DMARQ unless either the BUSY bit, the DRQ bit, or both are set to one.

Bit 6 (RDY): RDY indicates whether the device is capable of performing CompactFlash Storage Card operations. This bit is cleared at power up and remains cleared until the CompactFlash Storage Card is ready to accept a command.

Bit 5 (DWF): This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC): This bit is set when the CompactFlash Storage Card is ready.

Bit 3 (DRQ): The Data Request is set when the CompactFlash Storage Card requires that information be transferred either to or from the host through the Data register.

During the data transfer of DMA commands, the Card shall not assert DMARQ unless either the BUSY bit, the DRQ bit, or both are set to one.

Bit 2 (CORR): This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX): This bit is always set to 0.

Bit 0 (ERR): This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands (such as Read Sectors and Write Sectors) that end with an error condition should have the address of the first sector in error in the command block registers.

6.1.5.9 Device Control Register (Address - 3F6h[376h]; Offset Eh)

This register is used to control the CompactFlash Storage Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X(0)	X(0)	X(0)	X(0)	X(0)	SW Rst	-IEn	0

Figure 53: Device Control Register

Bit 7: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 6: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 5: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 4: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 3: this bit is ignored by the CompactFlash Storage Card. The host software should set this bit to 0.

Bit 2 (SW Rst): this bit is set to 1 in order to force the CompactFlash Storage Card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA PC Card Card Configuration Registers (see Section 4.4.4 to 4.4.9) as a hardware Reset does. The Card remains in Reset until this bit is reset to '0.'

Bit 1 (-IEn): the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the CompactFlash Storage Card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit 0: this bit is ignored by the CompactFlash Storage Card.

6.1.5.10 Card (Drive) Address Register (Address 3F7h[377h]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Figure 54: Card (Drive) Address Register

Bit 7: this bit is unknown.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the CompactFlash Storage Card. Following are some possible solutions to this problem for the PCMCIA PC Card implementation:

1) Locate the CompactFlash Storage Card at a non-conflicting address, i.e. Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.

2) Do not install a Floppy and a CompactFlash Storage Card in the system at the same time.

3) Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7h/377h when a CompactFlash Storage Card is installed and conversely to tri-state D6-D0 of I/O address 3F7h/377h when a floppy controller is installed.

4) Do not use the CompactFlash Storage Card's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0h-1F7h, 3F6h (or 170h-177h, 176h) to the CompactFlash Storage Card or b) if provided use an additional Primary / Secondary configuration in the CompactFlash Storage Card which does not respond to accesses to I/O locations 3F7h and 377h. With either of these implementations, the host software shall not attempt to use information in the Drive Address Register.

Bit 6 (-WTG): this bit is 0 when a write operation is in progress; otherwise, it is 1.

Bit 5 (-HS3): this bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2): this bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1): this bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0): this bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1): this bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0): this bit is 0 when the drive 0 is active and selected.

6.2 CF-ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the CompactFlash Storage Cards. Commands are issued to the CompactFlash Storage Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 50: CF-ATA Command Set) of command acceptance, all dependent on the host not issuing commands unless the CompactFlash Storage Card is not busy (BSY=0). All commands listed in this specification shall be implemented. Commands can be implemented as “no operation” to meet this requirement. The Security Mode feature set (command codes F1, F2, F3, F4, F5, and F6) should not be implemented unless the device is intended to be used in an embedded, non-removable application. The Security Mode feature set was not designed for removable devices and certain problems may be encountered when using these commands in a removable application. This specification introduces some new commands and features. If these commands are used on an older CF card, an Invalid Command Error may occur.

- Upon receipt of a Class 1 command, the CompactFlash Storage Card sets BSY within 400 nsec.
- Upon receipt of a Class 2 command, the CompactFlash Storage Card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears BSY within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the CompactFlash Storage Card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec (assuming no re-assignments), and clears BSY within 400 nsec of setting DRQ.

6.2.1 CF-ATA Command Set

Table 50: CF-ATA Command Set summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the Task File for each.

Table 50: CF-ATA Command Set

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
1	Flush Cache	E7h	-	-	-	-	D	-
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Device	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Key Management Structure Read	B9 Feature 0-127	C	C	C	C	D C	-
1	Key Management Read Keying Material	B9 Feature 80	C	C	C	C	D C	-
2	Key Management Change Key Management Value	B9 Feature 81	C	C	C	C	D C	-
1	NOP	00h	-	-	-	-	D	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA	C8h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense	03h	-	-	-	-	D	-
1	Security Disable Password	F6h	-	-	-	-	D	-
1	Security Erase Prepare	F3h	-	-	-	-	D	-
1	Security Erase Unit	F4h	-	-	-	-	D	-
1	Security Freeze Lock	F5h	-	-	-	-	D	-
1	Security Set Password	F1h	-	-	-	-	D	-
1	Security Unlock	F2h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Standby	E2h or 96h	-	-	-	-	D	-
1	Standby Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write DMA	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

Definitions:

- FR = Features Register
- SC = Sector Count Register
- SN = Sector Number Register
- CY = Cylinder Registers
- DH = Card/Drive/Head Register
- LBA = Logical Block Address Mode Supported (see command descriptions for use).
- Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Storage Card and head parameters are used; D - only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command descriptions for use).

6.2.1.1 Check Power Mode - 98h or E5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 55: Check Power Mode

This command checks the power mode.

If the CompactFlash Storage Card is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the CompactFlash Storage Card is in Idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

6.2.1.2 Execute Drive Diagnostic - 90h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 56: Execute Drive Diagnostic

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card.

When the diagnostic command is issued in a PCMCIA PC Card configuration mode, this command runs only on the CompactFlash Storage Card that is addressed by the Drive/Head register. This is because the PCMCIA PC Card interface does not allows for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in Table 51: Diagnostic Codes are returned in the Error Register at the end of the command.

Table 51: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

6.2.1.3 Erase Sector(s) - C0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 57: Erase Sector

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

6.2.1.4 Flush Cache – E7h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 58: Flush Cache

This command causes the card to complete writing data from its cache. The card returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the Compact Flash Storage Card does not support the Flush Cache command, the Compact Flash Storage Card shall return command aborted.

6.2.1.5 Format Track - 50h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

Figure 59: Format Track

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

6.2.1.6 Identify Device – ECh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 60: Identify Device

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 52. All reserved bits or words are zero. Hosts should not depend on Obsolete words in Identify Device containing 0. Table 52 specifies each field in the data returned by the Identify Device Command. In Table 52, X indicates a numeric nibble value specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 52: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the CompactFlash Storage Card
	0XXX	2	General configuration – Bit Significant with ATA-4 definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	XXXXh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
49	XX00h	2	Capabilities
50	0000h	2	Reserved
51	0X00h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	000Xh	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0X0Xh	2	Multiword DMA transfer. In PC Card modes this value shall be 0h
64	00XXh	2	Advanced PIO modes supported
65	XXXXh	2	Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h
66	XXXXh	2	Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h
67	XXXXh	2	Minimum PIO transfer cycle time without flow control
68	XXXXh	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	XXXXh	6	Features/command sets supported
85-87	XXXXh	6	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode Supported and Selected
89	XXXXh	2	Time required for Security erase unit completion
90	XXXXh	2	Time required for Enhanced security erase unit completion
91	XXXXh	2	Current Advanced power management value
92-127	0000h	72	Reserved
128	XXXXh	2	Security status
129-159	0000h	64	Vendor unique bytes
160	XXXXh	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	XXXXh	2	CF Advanced True IDE Timing Mode Capability and Setting
164	XXXXh	2	CF Advanced PC Card I/O and Memory Timing Mode Capability
165-167	0000h	6	Reserved for assignment by the CFA

Word Address	Default Value	Total Bytes	Data Field Type Information
168-255	0000h	158	Reserved

6.2.1.6.1 Word 0: General Configuration

This field indicates the general characteristics of the device. When Word 0 of the Identify drive information is 848Ah then the device is a CompactFlash Storage Card and complies with the CFA specification and CFA command set. It is recommended that PC Card modes of operation report only the 848Ah value as they are always intended as removable devices.

Bits 15-0: CF Standard Configuration Value
Word 0 is 848Ah. This is the recommended value of Word 0.

Some operating systems require Bit 6 of Word 0 to be set to 1 (Non-removable device) to use the card as the root storage device. The Card must be the root storage device when a host completely replaces conventional disk storage with a CompactFlash Card in True IDE mode. To support this requirement and provide capability for any future removable media Cards, alternate handling of Word 0 is permitted.

Bits 15-0: CF Preferred Alternate Configuration Values
044Ah: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while preserving all Retired bits in the word.
0040h: This is the alternate value of Word 0 turns on ATA device and turns off Removable Media and Removable Device while zeroing all Retired bits in the word

Bit 15-12: Configuration Flag
If bits 15:12 are set to 8h then Word 0 shall be 848Ah.
If bits 15:12 are set to 0h then Bits 11:0 are set using the definitions below and the Card is required to support for the CFA command set and report that in bit 2 of Word 83.
Bit 15:12 values other than 8h and 0h are prohibited.

Bits 11-8: Retired
These bits have retired ATA bit definitions. It is recommended that the value of these bits be either the preferred value of 0h or the value of 4h that preserves the corresponding bits from the 848Ah CF signature value.

Bit 7: Removable Media Device
If Bit 7 is set to 1, the Card contains media that can be removed during Card operation.
If Bit 7 is set to 0, the Card contains nonremovable media.

Bit 6: Not Removable Controller and/or Device
Alert! This bit will be considered for obsolescence in a future revision of this standard.
If Bit 6 is set to 1, the Card is intended to be nonremovable during operation.
If Bit 6 is set to 0, the Card is intended to be removable during operation.

Bits 5-0: Retired/Reserved
Alert! Bit 2 will be considered for definition in a future revision of this standard and shall be 0 at this time.
Bits 5-1 have retired ATA bit definitions.
Bit 2 shall be 0.
Bit 0 is Reserved and shall be 0.
It is recommended that the value of bits 5-0 be either the preferred value of 00h or the value of 0Ah that preserves the corresponding bits from the 848Ah CF signature value.

6.2.1.6.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.2.1.6.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.2.1.6.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.2.1.6.5 Words 7-8: Number of Sectors per Card

This field contains the number of sectors per CompactFlash Storage Card. This double word value is also the first invalid address in LBA translation mode.

6.2.1.6.6 Words 10-19: Serial Number

This field contains the serial number for this CompactFlash Storage Card and is right justified and padded with spaces (20h).

6.2.1.6.7 Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h.

6.2.1.6.8 Words 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

6.2.1.6.9 Words 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.2.1.6.10 Word 47: Read/Write Multiple Sector Count

Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the CompactFlash Storage Card supports for Read/Write Multiple commands.

6.2.1.6.11 Word 49: Capabilities

Bit 13: Standby Timer
If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command
If bit 13 is set to 0 then the Standby timer operation is defined by the vendor.

Bit 11: IORDY Supported

If bit 11 is set to 1 then this CompactFlash Storage Card supports IORDY operation.
If bit 11 is set to 0 then this CompactFlash Storage Card may support IORDY operation.

Bit 10: IORDY may be disabled
Bit 10 shall be set to 0, indicating that IORDY may not be disabled.

Bit 9: LBA supported
Bit 9 shall be set to 1, indicating that this CompactFlash Storage Card supports LBA mode addressing. CF devices shall support LBA addressing.

Bit 8: DMA Supported
If bit 8 is set to 1 then Read DMA and Write DMA commands are supported.
If bit 8 is set to 0, then Read DMA and Write DMA commands are not supported.

6.2.1.6.12 Word 51: PIO Data Transfer Cycle Timing Mode

The PIO transfer timing for each CompactFlash Storage Card falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

6.2.1.6.13 Word 53: Translation Parameters Valid

Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors.

If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any CompactFlash Storage Card that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

Bit 2 shall be set to 1 indicating that word 88 is valid and reflects the supported True IDE UDMA transfer modes.

6.2.1.6.14 Words 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.2.1.6.15 Words 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

6.2.1.6.16 Word 59: Multiple Sector Setting

Bits 15-9 are reserved and shall be set to 0.

Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid.

Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

6.2.1.6.17 Words 60-61: Total Sectors Addressable in LBA Mode

This field contains the total number of user addressable sectors for the CompactFlash Storage Card in LBA mode only.

6.2.1.6.18 Word 63: Multiword DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the CompactFlash Storage Card to indicate the multiword DMA mode which is currently selected.

Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.

Selection of Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163 as described in section 6.2.1.6.33: Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the Multiword DMA modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the CompactFlash Storage Card supports Multiword DMA modes 2, 1 and 0.

Support for Multiword DMA modes 3 and above are specific to CompactFlash are reported in word 163 as described in section 6.2.1.6.33: Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

6.2.1.6.19 Word 64: Advanced PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate the advanced PIO modes it is capable of supporting.

Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the CompactFlash Storage Card supports PIO mode 3. Bit 1, if set to one, indicates that the CompactFlash Storage Card supports PIO mode 4.

Support for PIO modes 5 and above are specific to CompactFlash are reported in word 163 as described in section 6.2.1.6.33: Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings.

6.2.1.6.20 Word 65: Minimum Multiword DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

6.2.1.6.21 Word 66: Recommended Multiword DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the CompactFlash Storage Card will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all CompactFlash Storage Cards supporting DMA modes 1 and above.

If bit 1 of word 53 is set to one, but this field is not supported, the Card shall return a value of zero in this field.

6.2.1.6.22 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash Storage Card guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field.

6.2.1.6.23 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the CompactFlash Storage Card supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any CompactFlash Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the CompactFlash Storage Card.

If bit 1 of word 53 is set to one because a CompactFlash Storage Card supports a field in words 64-70 other than this field and the CompactFlash Storage Card does not support this field, the CompactFlash Storage Card shall return a value of zero in this field.

6.2.1.6.24 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.

If bit 1 of word 82 is set to one, the Security Mode feature set is supported.

Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.

If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported.

Bit 7 of word 82 shall be set to zero; release interrupt is not supported.

Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.

Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 82 is obsolete.

Bit 12 of word 82 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command.

Bit 13 of word 82 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command.

Bit 14 of word 82 shall be set to one; the CompactFlash Storage Card supports the NOP command.

Bit 15 of word 82 is obsolete.

Bit 0 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Download Microcode command.

Bit 1 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands.

Bit 2 of word 83 shall be set to one; the CompactFlash Storage Card supports the CFA feature set.

If bit 3 of word 83 is set to one, the CompactFlash Storage Card supports the Advanced Power Management feature set.

Bit 4 of word 83 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set.

6.2.1.6.25 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by CompactFlash Storage Cards prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.

If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command.

Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.

Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.

Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.

If bit 5 of word 85 is set to one, write cache is enabled.

If bit 6 of word 85 is set to one, look-ahead is enabled.

Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.

Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.

Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.

Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.

Bit 11 of word 85 is obsolete.

Bit 12 of word 85 shall be set to one; the CompactFlash Storage Card supports the Write Buffer command.

Bit 13 of word 85 shall be set to one; the CompactFlash Storage Card supports the Read Buffer command.

Bit 14 of word 85 shall be set to one; the CompactFlash Storage Card supports the NOP command.

Bit 15 of word 85 is obsolete.

Bit 0 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Download Microcode command.

Bit 1 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Read DMA Queued and Write DMA Queued commands.

If bit 2 of word 86 shall be set to one, the CompactFlash Storage Card supports the CFA feature set.

If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.

Bit 4 of word 86 shall be set to zero; the CompactFlash Storage Card does not support the Removable Media Status feature set.

6.2.1.6.26 Word 88: True IDE Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported. Word 88 shall return a value of 0 if the device is not in True IDE mode or if it does not support UDMA in True IDE Mode.

Bit 15: Reserved

Bit 14: 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected

Bit 13: 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected

Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected

Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected

Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected

Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected

Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected

Bit 7: Reserved

Bit 6: 1 = Ultra DMA mode 6 and below are supported. Bits 0-5 Shall be set to 1.

Bit 5: 1 = Ultra DMA mode 5 and below are supported. Bits 0-4 Shall be set to 1.

Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 Shall be set to 1.

Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 Shall be set to 1.

Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 Shall be set to 1.

Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 Shall be set to 1.

Bit 0: 1 = Ultra DMA mode 0 is supported

6.2.1.6.27 Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete. This command shall be supported on CompactFlash Storage Cards that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

6.2.1.6.28 Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete. This command shall be supported on CompactFlash Storage Cards that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

6.2.1.6.29 Word 91: Advanced power management level value

Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

6.2.1.6.30 Word 128: Security Status

Bit 8: Security Level
If set to 1, indicates that security mode is enabled and the security level is maximum.
If set to 0 and security mode is enabled, indicates that the security level is high.

Bit 5: Enhanced security erase unit feature supported
If set to 1, indicates that the Enhanced security erase unit feature set is supported.

Bit 4: Expire
If set to 1, indicates that the security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset.

Bit 3: Freeze
If set to 1, indicates that the security is Frozen.

Bit 2: Lock
If set to 1, indicates that the security is locked.

Bit 1: Enable/Disable
If set to 1, indicates that the security is enabled.
If set to 0, indicates that the security is disabled.

Bit 0: Capability
If set to 1, indicates that CompactFlash Storage Card supports security mode feature set.
If set to 0, indicates that CompactFlash Storage Card does not support security mode feature set.

6.2.1.6.31 Word 160: Power Requirement Description

This word is required for CompactFlash Storage Cards that support power mode 1.

Bit 15: VLD
If set to 1, indicates that this word contains a valid power requirement description.
If set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV
This bit is reserved and shall be 0.

Bit 13: -XP
If set to 1, indicates that the CompactFlash Storage Card does not have Power Level 1 commands.
If set to 0, indicates that the CompactFlash Storage Card has Power Level 1 commands

Bit 12: -XE
If set to 1, indicates that Power Level 1 commands are disabled.
If set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current
This field contains the CompactFlash Storage Card's maximum current in mA.

6.2.1.6.32 Word 162: Key Management Schemes Supported

Bit 0: CPRM support
If set to 1, the device supports CPRM Scheme (Content Protection for Recordable Media)
If set to 0, the device does not support CPRM.

Bits 1-15 are reserved for future additional Key Management schemes.

6.2.1.6.33 Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings

This word describes the capabilities and current settings for CFA defined advanced timing modes using the True IDE interface.

Notice! The use of True IDE PIO Modes 5 and above or of Multiword DMA Modes 3 and above impose significant restrictions on the implementation of the host as indicated in section 4.3.7: Additional Requirements for CF Advanced Timing Modes.

There are four separate fields defined that describe support and selection of Advanced PIO timing modes and Advanced Multiword DMA timing modes. The older modes are reported in words 63 and 64 as described in sections 6.2.1.6.18: Word 63: Multiword DMA transfer and 6.2.1.6.19: Word 64: Advanced PIO transfer modes supported.

Bits 2-0: Advanced True IDE PIO Mode Support
Indicates the maximum True IDE PIO mode supported by the card.

Value	Maximum PIO mode timing supported
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 5-3: Advanced True IDE Multiword DMA Mode Support
Indicates the maximum True IDE Multiword DMA mode supported by the card.

Value	Maximum Multiword DMA timing mode supported
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 8-6: Advanced True IDE PIO Mode Selected
Indicates the current True IDE PIO mode selected on the card.

Value	Current PIO timing mode selected
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 11-9: Advanced True IDE Multiword DMA Mode Selected
Indicates the current True IDE Multiword DMA Mode Selected on the card.

Value	Current Multiword DMA timing mode selected
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 15-12 are reserved.

6.2.1.6.34 Word 164: CF Advanced PC Card I/O and Memory Timing Modes Capabilities and Settings

This word describes the capabilities and current settings for CFA defined advanced timing modes using the Memory and PC Card I/O interface.

Notice! The use of PC Card I/O or Memory modes that are 100ns or faster impose significant restrictions on the implementation of the host as indicated in section 4.3.7: Additional Requirements for CF Advanced Timing Modes.

Bits 2-0: Maximum Advanced PC Card I/O Mode Support
Indicates the maximum I/O timing mode supported by the card.

Value	Maximum PC Card IO timing mode supported
0	255 ns Cycle PC Card I/O Mode
1	120 ns Cycle PC Card I/O Mode
2	100 ns Cycle PC Card I/O Mode
3	80 ns Cycle PC Card I/O Mode
4-7	Reserved

Bits 5-3: Maximum Memory timing mode supported
Indicates the Maximum Memory timing mode supported by the card.

Value	Maximum Memory timing mode Supported
0	250 ns Cycle Memory Mode
1	120 ns Cycle Memory Mode
2	100 ns Cycle Memory Mode
3	80 ns Cycle Memory Mode
4-7	Reserved

Bits 8-6: Maximum PC Card I/O UDMA timing mode supported
Indicates the Maximum PC Card I/O UDMA timing mode supported by the card when bit 15 is set.

Value	Maximum PC Card I/O UDMA timing mode Supported
0	PC Card I/O UDMA mode 0 supported
1	PC Card I/O UDMA mode 1 supported
2	PC Card I/O UDMA mode 2 supported
3	PC Card I/O UDMA mode 3 supported
4	PC Card I/O UDMA mode 4 supported
5	PC Card I/O UDMA mode 5 supported
6	PC Card I/O UDMA mode 6 supported
7	Reserved

Bits 11-9: Maximum PC Card Memory UDMA timing mode supported
Indicates the Maximum PC Card Memory UDMA timing mode supported by the card when bit 15 is set.

Value	Maximum PC Card Memory UDMA timing mode Supported
0	PC Card Memory UDMA mode 0 supported
1	PC Card Memory UDMA mode 1 supported
2	PC Card Memory UDMA mode 2 supported
3	PC Card Memory UDMA mode 3 supported
4	PC Card Memory UDMA mode 4 supported
5	PC Card Memory UDMA mode 5 supported
6	PC Card Memory UDMA mode 6 supported
7	Reserved

Bits 14-12: PC Card Memory or I/O UDMA timing mode selected
Indicates the PC Card Memory or I/O UDMA timing mode selected by the card.

Value	PC Card Memory or I/O UDMA timing mode Selected
0	PC Card I/O UDMA mode 0 selected
1	PC Card I/O UDMA mode 1 selected
2	PC Card I/O UDMA mode 2 selected
3	PC Card I/O UDMA mode 3 selected
4	PC Card I/O UDMA mode 4 selected
5	PC Card I/O UDMA mode 5 selected
6	PC Card I/O UDMA mode 6 selected
7	Reserved

Bit 15: PC Card Memory and IO Modes Supported

This bit, when set, indicates that the PC Card UDMA support values in bits 11-6 are valid. When this bit is cleared, PC Card Memory and IO Modes are not supported by the device.

6.2.1.7 Idle - 97h or E3h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

Figure 61: Idle

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

6.2.1.8 Idle Immediate - 95h or E1h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95h or E1h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 62: Idle Immediate

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

6.2.1.9 Initialize Drive Parameters - 91h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91h							

C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)
Cyl High (5)	X				
Cyl Low (4)	X				
Sec Num (3)	X				
Sec Cnt (2)	Number of Sectors				
Feature (1)	X				

Figure 63: Initialize Drive Parameters

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

6.2.1.10 Key Management Structure Read – B9h (Feature: 0-127)

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B9h							
C/D/H (6)	Reserved (0)			Drive	Reserved (0)			
Cyl High (5)	C7-0							
Cyl Low (4)	C15-8							
Sec Num (3)	C23-16							
Sec Cnt (2)	C31-24							
Feature (1)	0	C38-32						

Figure 64: Key Management Structure Read

The KEY MANAGEMENT STRUCTURE READ command is optional, depending on the Key Management scheme in use.

This command returns a 512-byte Key Management data structure via PIO data-in transfer. The structure encodes device Key Management status defined by the Key Management scheme in use. In some schemes, this structure may include a cryptographic response.

The values 39-bit value C38-0 is a random number picked by the host. It is used as a challenge value by some Key Management schemes. All 39-bit values are acceptable.

6.2.1.11 Key Management Read Keying Material - B9h (Feature: 80)

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B9h							
C/D/H (6)	Reserved (0)			Drive	Reserved (0)			
Cyl High (5)	Reserved (0)							
Cyl Low (4)	Keying Material Sector Offset - High							
Sec Num (3)	Keying Material Sector Offset - Low							
Sec Cnt (2)	Keying Material Count							
Feature (1)	80h							

Figure 65: Key Management Read Keying Material

The KEY MANAGEMENT READ KEYING MATERIAL command is optional, depending on the Key Management scheme in use.

This command reads from 1 to 256 sectors as specified in the Sector Count register. A Sector Count of 0 requests 256 sectors. The transfer shall begin at the Sector Offset within the keying material specified in the 16 bit number comprised of the Sector Number and Cylinder Low registers. The size and format of the keying material is specific to the Key Management scheme in use.

If an uncorrectable error occurs reading the keying material, the Sector Number and Cylinder Low registers are left indicating the offset of the sector in error.

6.2.1.12 Key Management Change Key Management Value – B9h (Feature: 81)

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B9h							
C/D/H (6)	Reserved (0)			Drive	Reserved (0)			
Cyl High (5)	B2h							
Cyl Low (4)	6Eh							
Sec Num (3)	Reserved (0)							
Sec Cnt (2)	Reserved (0)							
Feature (1)	81h							

Figure 66: Key Management Change Key Management Value

The KEY MANAGEMENT CHANGE KEY MANAGEMENT VALUE command is optional, depending on the Key Management scheme in use.

This command causes the device to change a value found in the KEY MANAGEMENT READ KEY MANAGEMENT STRUCTURE response. The method is specific to the Key Management scheme in use. The special value B26Eh in the cylinder registers is checked by the card to make it less likely that the command was executed by mistake.

6.2.1.13 NOP - 00h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	00h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 67: NOP

This command always fails with the CompactFlash Storage Card returning command aborted.

6.2.1.14 Read Buffer - E4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 68: Read Buffer

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.2.1.15 Read DMA – C8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 69: Read DMA

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the

error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

6.2.1.16 Read Long Sector - 22h or 23h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22h or 23h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 70: Read Long Sector

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the CompactFlash Storage Card does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

6.2.1.17 Read Multiple - C4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 71: Read Multiple

Note: This specification requires that CompactFlash Cards support a multiple block count of 1 and permits larger values to be supported.

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block, which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = (sector count) modulo (block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer shall take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

6.2.1.18 Read Sector(s) - 20h or 21h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 72: Read Sector(s)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the CompactFlash Storage Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

6.2.1.19 Read Verify Sector(s) - 40h or 41h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 73: Read Verify Sector(s)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY.

When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

6.2.1.20 Recalibrate - 1Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 74: Recalibrate

This command is effectively a NOP command to the CompactFlash Storage Card and is provided for compatibility purposes.

6.2.1.21 Request Sense - 03h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03h							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 75: Request Sense

This command requests extended error information for the previous command. Table 53 defines the valid extended error codes for the CompactFlash Storage Card Series product. The extended error code is returned to the host in the Error Register.

Table 53: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

6.2.1.22 Security Disable Password - F6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F6h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 76: Security Disable Password

This command requests a transfer of a single sector of data from the host. Table 54 defines the content of this sector of information. If the password selected by word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password. Use of this command is not recommended by the CFA.

Table 54: Security Password Data Content

Word	Content
0	Control word Bit 0: identifier 0=compare User password 1=compare Master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-256	Reserved

6.2.1.23 Security Erase Prepare - F3h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F3h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 77: Security Erase Prepare

This command shall be issued immediately before the Security Erase Unit command to enable device erasing and unlocking. This command prevents accidental erase of the CompactFlash Storage Card. Use of this command is not recommended by the CFA.

6.2.1.24 Security Erase Unit - F4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F4h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 78: Security Erase Unit

This command requests transfer of a single sector of data from the host. Table 54 defines the content of this sector of information. If the password does not match the password previously saved by the CompactFlash Storage Card, the CompactFlash Storage Card rejects the command with command aborted. The Security Erase Prepare command shall be completed immediately prior to the Security Erase Unit command. If the CompactFlash Storage Card receives a Security Erase Unit command without an immediately prior Security Erase Prepare command, the CompactFlash Storage Card command aborts the Security Erase Unit command. Use of this command is not recommended by the CFA.

6.2.1.25 Security Freeze Lock - F5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 79: Security Freeze Lock

The Security Freeze Lock command sets the CompactFlash Storage Card to Frozen mode. After command completion, any other commands that update the CompactFlash Storage Card Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security Freeze Lock is issued when the CompactFlash Storage Card is in Frozen mode, the command executes and the CompactFlash Storage Card remains in Frozen mode. After command completion, the Sector Count Register shall be set to 0. Use of this command is not recommended by the CFA.

Commands disabled by Security Freeze Lock are:

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

If security mode feature set is not supported, this command shall be handled as Wear Level command.

6.2.1.26 Security Set Password - F1h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F1h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 80: Security Set Password

This command requests a transfer of a single sector of data from the host. Table 55 defines the content of the sector of information. The data transferred controls the function of this command.

Table 56 defines the interaction of the identifier and security level bits. Use of this command is not recommended by the CFA.

Table 55: Security Set Password Data Content

Word	Content
0	Control word Bit 0: Identifier 0=set User password 1=set Master password Bits 1-7: Reserved Bit 8: Security level 0=High 1=Maximum Bits 9-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

Table 56: Identifier and Security Level Bit Interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The CompactFlash Storage Card shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new user password. The lock mode shall be enabled from the next power-on reset or hardware reset. The CompactFlash Storage Card shall then be unlocked by only the User password. The Master password previously set is still stored in the CompactFlash Storage Card shall not be used to unlock the CompactFlash Storage Card.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

6.2.1.27 Security Unlock - F2h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F2h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 81: Security Unlock

This command requests transfer of a single sector of data from the host. Table 54 defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in the maximum security level, then the unlock command shall be rejected. If the identifier bit is set to user, then the device compares the supplied password with the stored User password. If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when Security Unlock is issued and the device is locked. Once this counter reaches zero, the Security Unlock and Security Erase Unit commands are command aborted until after a power-on reset or a hardware reset is received. Security Unlock commands issued when the device is unlocked have no effect on the unlock counter. Use of this command is not recommended by the CFA.

6.2.1.28 Seek - 7Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 82: Seek

This command is effectively a NOP command to the CompactFlash Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.2.1.29 Set Features – EFh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

Figure 83: Set Features

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the Compact Flash Storage Card shall return command aborted. Table 57: Feature Supported defines all features that are supported.

Table 57: Feature Supported

Feature	Operation
01h	Enable 8 bit data transfers.
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Count register.
05h	Enable Advanced Power Management.
09h	Enable Extended Power operations. ***(Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)***
0Ah	Enable Power Level 1 commands.
44h	Product specific ECC bytes apply on Read/Write Long commands.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
82h	Disable Write Cache.
85h	Disable Advanced Power Management.
89h	Disable Extended Power operations***. (Alert: It has been proposed to remove this feature from a future revision of the specification. Please notify the CFA if you have a requirement for this feature.)***
8Ah	Disable Power Level 1 commands.
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers.

Features 02h and 82h allow the host to enable or disable write cache in CompactFlash Storage Cards that implement write cache. When the subcommand disable write cache is issued, the CompactFlash Storage Card shall initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Table 58: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b[1]	Mode[1]
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Notes: 1) Multiword DMA is not permitted for devices configured in the PC Card Memory or the PC Card I/O interface mode.

If a CompactFlash Storage Card supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of “00000000b”, it shall set its default PIO mode. If the value is “00000001b” and the CompactFlash Storage Card supports disabling of IORDY, then the CompactFlash Storage Card shall set its default PIO mode and disable IORDY. A CompactFlash Storage Card shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.

Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.

A CompactFlash Storage Card reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported. Note that Multiword DMA shall not be supported while PC Card interface modes are selected.

A CompactFlash Storage Card reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.

If an Ultra DMA mode is enabled, any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device. Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Table 59: Advanced power management levels shows these values.

Table 59: Advanced power management levels

Level	Sector Count Value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.

Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the CF+ CompactFlash Storage Card with extended power as they require Power Level 1 to perform their full set of functions.

Power Enhanced CF Storage Cards are required to power up and execute all supported commands and protocols in Power Level 0, Their default feature shall be 8Ah: Disable Power Level 1 Commands. No commands are actually excluded for such cards in Power Level 0 because no commands require Power Level 1. The 8Ah default allows the cards to restrict their operating power to Power Level 0 limits for compatibility with hosts that do not recognize or support the extended power capabilities of Power Enhanced CF Storage Cards. It also allows hosts that support extended power to take advantage of it by setting the feature to 0Ah: Enable Power Level 1 Commands.

Features 55h and BBh are the default features for the CompactFlash Storage Card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register were set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

6.2.1.30 Set Multiple Mode - C6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							

Sec Cnt (2)	Sector Count
Feature (1)	X

Figure 84: Set Multiple Mode

This command enables the CompactFlash Storage Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash Storage Card sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the block count is not supported, an Aborted Command error is posted and the Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

6.2.1.31 Set Sleep Mode- 99h or E6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 85: Set Sleep Mode

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

6.2.1.32 Standby - 96h or E2h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96h or E2h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 86: Standby

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.2.1.33 Standby Immediate - 94h or E0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94h or E0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 87: Standby Immediate

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.2.1.34 Translate Sector - 87h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 88: Translate Sector

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 60 represents the information in the buffer. Please note that this command is unique to the CompactFlash Storage Card.

Table 60: Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) [1]
1Bh-1FFh	Reserved

Notes 1) A value of 0 indicates Hot Count is not supported.

6.2.1.35 Wear Level - F5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

Figure 89: Wear Level

For the CompactFlash Storage Cards that do not support security mode feature set, this command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register shall always be returned with a 00h indicating Wear Level is not needed. If the CompactFlash Storage Card supports security mode feature set, this command shall be handled as Security Freeze Lock.

6.2.1.36 Write Buffer - E8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 90: Write Buffer

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

6.2.1.37 Write DMA – CAh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 91: Write DMA

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector written. If an error occurs, the write terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

When a Write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

6.2.1.38 Write Long Sector - 32h or 33h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 92: Write Long Sector

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state CompactFlash Storage Card, the four bytes of ECC transferred by the host may be used by the CompactFlash Storage Card. The CompactFlash Storage Card may discard these four bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

6.2.1.39 Write Multiple Command - C5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 93: Write Multiple Command

Note: This specification requires that CompactFlash Cards support a multiple block count of 1 and permits larger values to be supported.

This command is similar to the Write Sectors command. The CompactFlash Storage Card sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block that contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = (sector count) modulo (block count).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation shall be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector numbers of the sector where the error occurred. The Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

6.2.1.40 Write Multiple without Erase – CDh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 94: Write Multiple without Erase

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

6.2.1.41 Write Sector(s) - 30h or 31h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 95: Write Sector(s)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of

the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

6.2.1.42 Write Sector(s) without Erase - 38h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 96: Write Sector(s) without Erase

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

6.2.1.43 Write Verify - 3Ch

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 97: Write Verify

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

6.2.2 Error Posting

Table 61: Error and Status Register summarizes the valid status and error value for all the CF-ATA Command set.

Table 61: Error and Status Register

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic[1]						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Flush Cache				V		V	V	V		V
Format Track			V	V	V	V	V	V		V
Identify Device				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Key Management Structure Read		V	V	V		V		V		V
Key Management Read Keying Material		V	V	V		V		V		V
Key Management Change Key Management Value		V		V		V	V	V		V
NOP				V		V	V			V
Read Buffer				V		V	V	V		V
Read DMA	V	V	V	V	V	V	V	V	V	V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Security Disable Password				V		V	V	V		V
Security Erase Prepare				V		V	V	V		V
Security Erase Unit				V		V	V	V		V
Security Freeze Lock				V		V	V	V		V
Security Set Password				V		V	V	V		V
Security Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write DMA	V		V	V	V	V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

V = valid on this command

[1] See Table 51: Diagnostic Codes.

6.2.3 Key Management Feature Set

Support of the optional Key Management feature set is denoted by a non-zero word 162 in the IDENTIFY DEVICE response. Commands unique to the Key Management feature set use a single command code and are differentiated from one another by the value placed in the Features register. These commands are:

Table 62: Key Management Features register values

Value	Command
00h-7Fh	READ KEY MANAGEMENT STRUCTURE
80h	READ KEYING MATERIAL
81h	CHANGE KEY MANAGEMENT VALUE
82h-FFh	Reserved

The READ KEY MANAGEMENT STRUCTURE command returns device status relevant to a Key Management scheme. The details of the structure are specific to the given scheme. For the most part, this status is dynamic. In contrast, the READ KEYING MATERIAL command returns constant information that is set at manufacturing time using vendor-specific methods. This information is the keying material necessary for compliant hosts to calculate interoperable keys through the card's media. Its size and format is also specific to the given Key Management scheme in use.

The READ KEY MANAGEMENT STRUCTURE command has a built-in 39-bit challenge that is used by some Key Management schemes to authenticate the card.

The CHANGE KEY MANAGEMENT VALUE command is used to modify values that are found in the READ KEY MANAGEMENT STRUCTURE command's response.

CPRM is the only Key Management Scheme that has been adopted. See section 8.4 Bibliography for references to CPRM documentation. Additional schemes may be considered for future adoption as needed.

Other values of the Feature register and the Head field (bits 3-0) in the C/D/H register are reserved for the use of future Key Management schemes. Cards supporting only CPRM should abort if the Head field is other than 0.

6.2.4 Security Mode Feature Set

The Security Mode feature set allows a host to implement a security password system to prevent unauthorized access to the CompactFlash Storage Card. A device that implements the Security Mode feature set shall implement the following minimum set of commands:

- Security Set Password
- Security Unlock
- Security Erase Prepare
- Security Erase Unit
- Security Freeze Lock
- Security Disable Password

Support of the Security Mode feature set is indicated in Identify Device word 128. The Security Mode feature set (command codes F1, F2, F3, F4, F5, and F6) should not be implemented unless the device is intended to be used in an embedded, non-removable application. The Security Mode feature set was not designed for removable devices and certain problems may be encountered when using these commands in a removable application.

6.2.4.1 Security Mode Default Setting

The Master password shall be set to a vendor specific value during manufacturing and the Lock mode disabled. The system manufacturer/dealer may set a new Master password using the Security Set Password command, without enabling or disabling the Lock mode.

6.2.4.2 Initial Setting of the User Password

When a User password is set, the device shall automatically enter Lock mode the next time the device is powered-on or after a hardware reset.

6.2.4.3 Security Mode Operation from Power-On or Hardware Reset

When Lock is enabled, the device rejects media access commands until a Security Unlock command is successfully completed.

6.2.4.4 Frozen Mode

The Security Freeze Lock command places the device in Frozen mode. This prevents accidental or malicious password activation or setting. Table 63: Security Mode Command Actions lists the

commands that the device shall be able to execute when in Frozen mode. The device shall exit Frozen mode on power off. All devices that support the Security Mode feature set should be issued a Security Freeze Lock command during system initialization.

6.2.4.5 User Password Lost

If the User password does not match and High level security is set, the device shall not allow the user to access data. The device shall be unlocked using the Master password. If the User password is lost and Maximum security level is set, data access shall not be allowed. However, the Security Erase Unit command shall unlock the device and shall erase all user data if the Master password matches.

6.2.4.6 Attempt Limit for SECURITY UNLOCK Command

The device shall have an attempt limit counter. The purpose of this counter is to defeat repeated trial attacks. After each failed User or Master password Security Unlock command, the counter is decremented. When the counter value reaches zero the Expire bit (bit 4) of word 128 in the Identify Device information is set, and the Security Unlock and Security Unit Erase commands are command aborted until the device is powered off or hardware reset. The Expire bit shall be cleared to zero after power on or hardware reset. The counter shall be set to five after a power on or hardware reset.

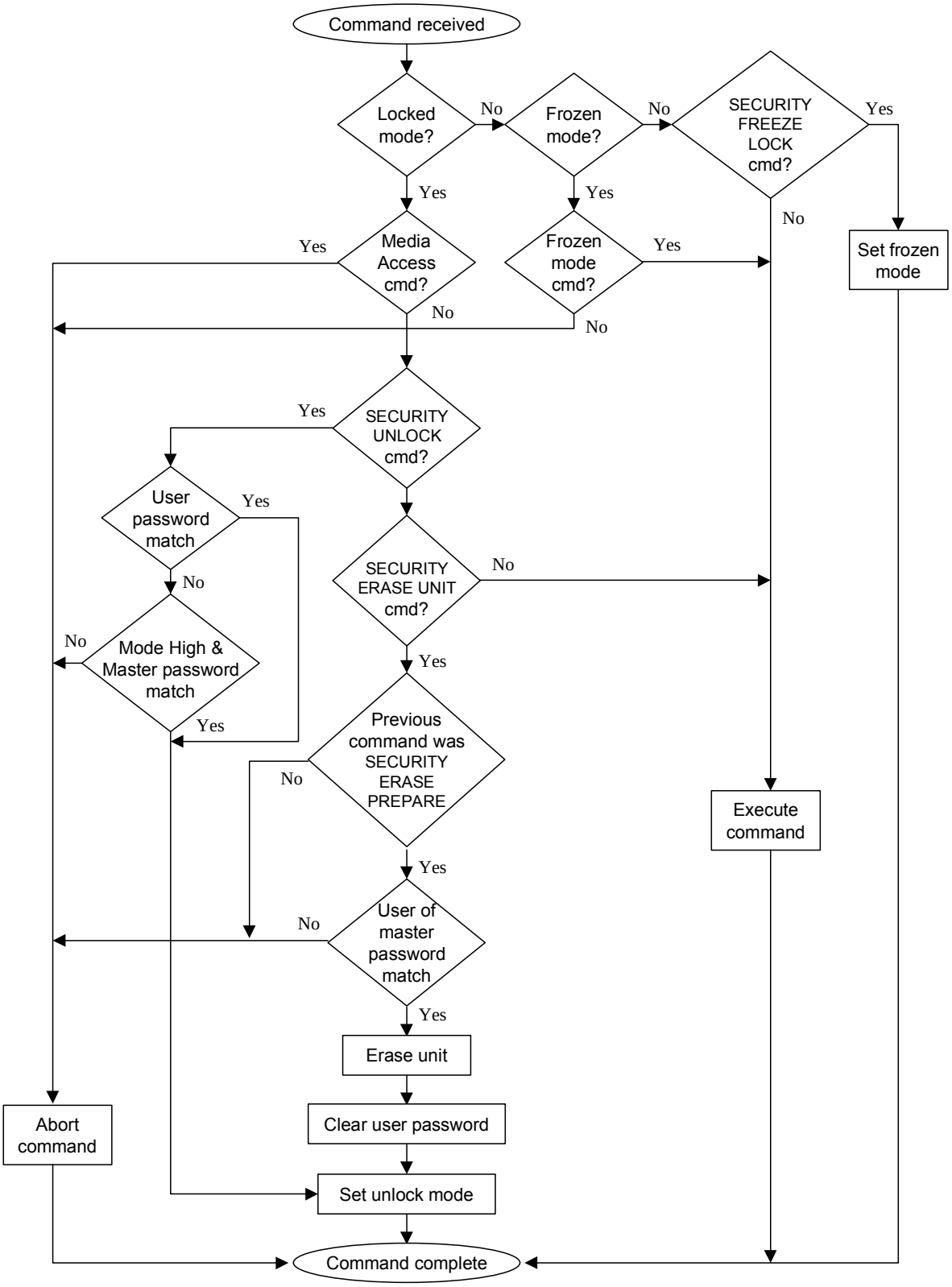


Figure 98: Security Mode Flow

Table 63: Security Mode Command Actions

Command	Locked	Unlocked	Frozen
Check Power Mode	Executable	Executable	Executable
Execute Drive Diagnostic	Executable	Executable	Executable
Erase Sector(s)	Command aborted	Executable	Executable
Flush Cache	Command aborted	Executable	Executable
Format Track	Command aborted	Executable	Executable
Identify Device	Executable	Executable	Executable
Idle	Executable	Executable	Executable
Idle Immediate	Executable	Executable	Executable
Initialize Drive Parameters	Executable	Executable	Executable
NOP	Executable	Executable	Executable
Read Buffer	Executable	Executable	Executable
Read Multiple	Command aborted	Executable	Executable
Read Long Sector	Command aborted	Executable	Executable
Read Sector(s)	Command aborted	Executable	Executable
Read Verify Sectors	Command aborted	Executable	Executable
Recalibrate	Executable	Executable	Executable
Request Sense	Executable	Executable	Executable
Security Disable Password	Command aborted	Executable	Command aborted
Security Erase Prepare	Executable	Executable	Command aborted
Security Erase Unit	Executable	Executable	Command aborted
Security Freeze Lock	Command aborted	Executable	Executable
Security Set Password	Command aborted	Executable	Command aborted
Security Unlock	Executable	Executable	Command aborted
Seek	Executable	Executable	Executable
Set Features	Executable	Executable	Executable
Set Multiple Mode	Executable	Executable	Executable
Set Sleep Mode	Executable	Executable	Executable
Stand By	Executable	Executable	Executable
Stand By Immediate	Executable	Executable	Executable
Translate Sector	Executable	Executable	Executable
Wear Level	Executable	Executable	Executable
Write Buffer	Executable	Executable	Executable
Write Long Sector	Command aborted	Executable	Executable
Write Multiple	Command aborted	Executable	Executable
Write Multiple w/o Erase	Command aborted	Executable	Executable
Write Sector(s)	Command aborted	Executable	Executable
Write Sector(s) w/o Erase	Command aborted	Executable	Executable
Write Verify	Command aborted	Executable	Executable

7 CompactFlash Adapters

7.1 Overview

CompactFlash and CF+ Type I products can be used with a PCMCIA Type II passive adapters. This adapter converts the Type I CompactFlash Storage Card or CF+ Card into a Type II PCMCIA PC card.

CompactFlash and CF+ Type II products can be used with PCMCIA Type II passive adapters. This adapter converts the Type II CompactFlash Storage Card or CF+ Card into a Type II PCMCIA PC card.

CF adapters shall physically and electrically conform to the PCMCIA PC Card Standard.

7.2 CompactFlash Adapter Specifications

The following subsections describe the Type I and Type II CompactFlash Adapters.

7.2.1 Specification applying to all CompactFlash Adapters

7.2.1.1 CompactFlash Adapter Overall Mechanical Dimensions

Refer to Table 64, Figure 100 and Figure 101 for the CompactFlash Adapter physical specifications.

Table 64: CompactFlash Adapter Physical Specifications

Length:	85.6 ± 0.20 mm (3.370 ±.008 in)
Width:	54.0 ± 0.10 mm (2.126 ± .004 in)
Thickness:	5.0 mm max. (0.1968 in)

7.2.1.2 CompactFlash Adapter Card Resistance

When measured between the solder lead pad on the 50 position straddle mount header and the solder lead pad on the 68 position receptacle, there should be 150 milliohms maximum bulk resistance per circuit.

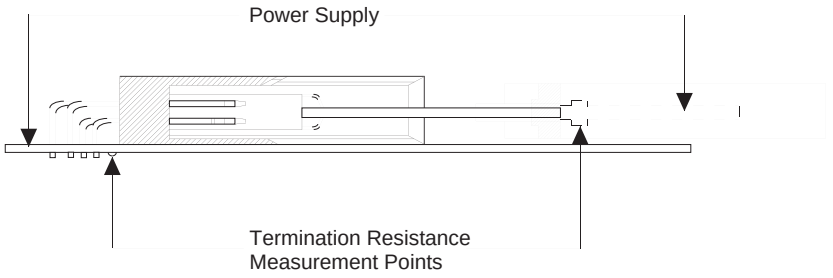


Figure 99: Termination Resistance Measurement Points

7.2.1.3 Ground Clip & Resistance

The CF to PC Card Adapter should have two ground clips, one on each side to support I/O cards that utilize ground clips. If the ground clips are present on the Adapter, the remainder of this section shall apply.

The size and dimension of the ground clips are not defined, only that they shall meet the PCMCIA specification in terms of resistance. The contact resistance as specified in the PCMCIA Card Physical section 6.1 shall be adopted in its entirety. The ground clips on the CF Type II and CF+ are specified in the card physical.

The contact resistance path is measured from the center of the PC Card nearest 68 pin connector (Test Point A) to the center of the CompactFlash card at the rear (Test Point B).

Table 65: Termination Resistance Procedure

Test Description	Requirement	Procedure
Termination Resistance	Initial: Signal, 260 milliohms maximum. Ground, 100 milliohms maximum. ΔR 20 milliohms maximum.	Subject samples to 50 mV maximum open circuit at 100 mA maximum.

7.2.2 Type I CompactFlash Adapter Diagram

Type I CompactFlash Adapters are used to adapt Type I CompactFlash and CF+ cards for use in Type II (5 mm thick) PCMCIA card slots. The mechanical drawing for Type I adapters appears in Figure 100: Type I CompactFlash Adapter.

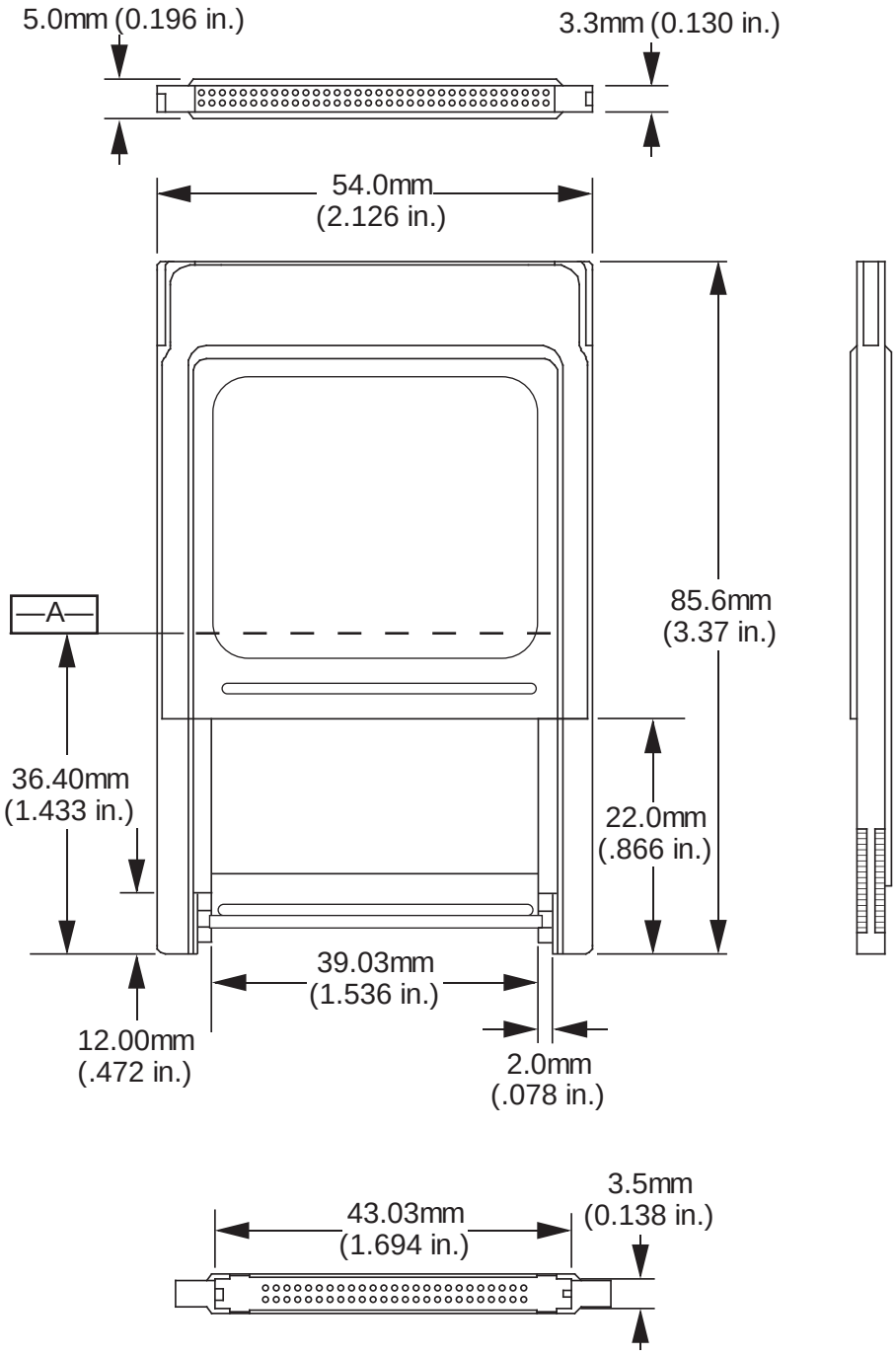


Figure 100: Type I CompactFlash Adapter

7.2.3 Type II CompactFlash Adapter Specifications

Type II CompactFlash Adapters are used to adapt Type II CompactFlash and CF+ cards for use in Type II (5 mm thick) PCMCIA card slots. The diagram for these adapters is show below and the other specifications are presented in the following subsections.

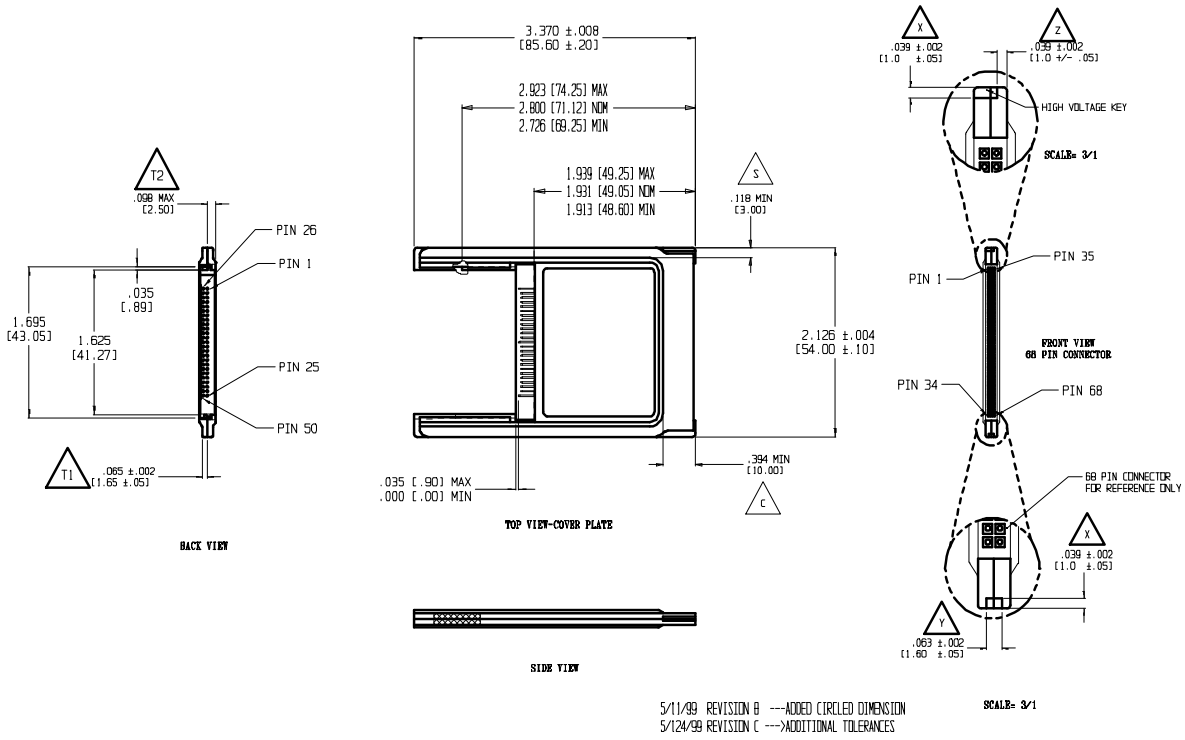


Figure 101: Type II CompactFlash Adapter

7.2.3.1 Shutter Mechanism

The Shutter Mechanism is defined as a protective device or shield for the 50 pin host pins. The shutter, in its fully extended position, shall not exceed .035 in. [.90 mm] max or 0.00 in. [0.00 MM] min from the longest pin.

7.2.3.2 Position of CompactFlash Type II Card

The CF Type II standard length Card, when fully inserted to the PC Card adapter, shall be flush with the rear of the Adapter. The CF Type II standard length Card shall not protrude past the PCMCIA PC Card Type II specification, nor shall it be recessed when inserted into the PC Card Adapter.

7.2.3.3 Mating and Unmating Force

See Table 3: Connector Interface Requirement- Total Mating Force and Total Unmating Force.

7.2.3.4 Key / Rail Length

The rail length is specified as **69.25 mm Minimum to 74.25 mm Maximum.** The purpose is to improve stability of the CF Type II Card to the PC Card Type II Adapter.

7.2.3.5 Force to Overcome Shutter Locking Mechanism

The shutter mechanism is designed with a lock to prevent movement of the shutter when the CF Type II Card is not engaged. This lock is to prevent pin damage to the 50 host pins. The force to overcome this mechanism is specified as **29.4N Minimum**

7.2.3.6 Shutter Force

The amount of force necessary to move the shutter mechanism, once the shutter lock mechanism has been disengaged is not to exceed the minimum Unmating force of the 50 pin host connector: **4.9N Maximum**.

7.3 Electrical Differences Between the CompactFlash Storage/CF+ Card and the CompactFlash Adapter

The CompactFlash Storage Card and the CompactFlash CF+ Card are electrically compatible with the CompactFlash Adapter. When a CompactFlash or CF+ card is installed in a CompactFlash adapter, the combination conforms to the PCMCIA PC Card Standard. CompactFlash products use a 50 pin connector and CompactFlash Adapters use a 68 pin connector. Both connectors use less than 50 signals. Table 50 shows the pinout differences between the CompactFlash Storage/CF+ Card and the CompactFlash Adapter.

Table 66: Pinout Differences Between CF Storage Card and CF Adapter

CF Adapter 68 Pin	68 Pin Pin #	50 Pin Pin #	CF Storage/ CF+ Card 50 Pin	CF Adapter 68 Pin	68 Pin Pin #	50 Pin Pin #	CF Storage/ CF+ Card 50 Pin
GND	Pin 1	Pin 1	GND	GND	Pin 35	Pin 1	GND
D03	Pin 2	Pin 2	D03	-CD1	Pin 36	Pin 26	-CD1
D04	Pin 3	Pin 3	D04	D11	Pin 37	Pin 27	D11
D05	Pin 4	Pin 4	D05	D12	Pin 38	Pin 28	D12
D06	Pin 5	Pin 5	D06	D13	Pin 39	Pin 29	D13
D07	Pin 6	Pin 6	D07	D14	Pin 40	Pin 30	D14
-CE1	Pin 7	Pin 7	-CE1 (-CS0)	D15	Pin 41	Pin 31	D15
A10	Pin 8	Pin 8	A10	-CE2	Pin 42	Pin 32	-CE2 (-CS1)
-OE	Pin 9	Pin 9	-OE (_ATA SEL)	-VS1	Pin 43	Pin 33	-VS1
A11	Pin 10			-IORD	Pin 44	Pin 34	-IORD
A09	Pin 11	Pin 10	A09	-IOWR	Pin 45	Pin 35	-IOWR
A08	Pin 12	Pin 11	A08	A17	Pin 46		
A13	Pin 13			A18	Pin 47		
A14	Pin 14			A19	Pin 48		
-WE	Pin 15	Pin 36	-WE	A20	Pin 49		
READY / -IREQ	Pin 16	Pin 37	READY / -IREQ (INTRQ)	A21	Pin 50		
VCC	Pin 17	Pin 13	VCC	VCC	Pin 51	Pin 38	VCC
VPP1	Pin 18			VPP2	Pin 52		
A16	Pin 19			A22	Pin 53		
A15	Pin 20			A23	Pin 54		
A12	Pin 21			A24	Pin 55		
A07	Pin 22	Pin 12	A07	A25	Pin 56	Pin 39	CSEL
A06	Pin 23	Pin 14	A06	-VS2	Pin 57	Pin 40	-VS2
A05	Pin 24	Pin 15	A05	RESET	Pin 58	Pin 41	RESET (-RESET)
A04	Pin 25	Pin 16	A04	-WAIT	Pin 59	Pin 42	-WAIT (IOREADY)
A03	Pin 26	Pin 17	A03	-INPACK	Pin 60	Pin 43	-INPACK (-DMARQ^{D})
A02	Pin 27	Pin 18	A02	-REG	Pin 61	Pin 44	-REG (DMACK^{D})
A01	Pin 28	Pin 19	A01	BVD2 / -SPKR	Pin 62	Pin 45	BVD2 / -SPKR (-DASP)
A00	Pin 29	Pin 20	A00	BVD1 / -STSCHG	Pin 63	Pin 46	BVD1 / -STSCHG (-PDIAG)

CF Adapter 68 Pin	68 Pin Pin #	50 Pin Pin #	CF Storage/ CF+ Card 50 Pin	CF Adapter 68 Pin	68 Pin Pin #	50 Pin Pin #	CF Storage/ CF+ Card 50 Pin
D00	Pin 30	Pin 21	D00	D08	Pin 64	Pin 47	D08
D01	Pin 31	Pin 22	D01	D09	Pin 65	Pin 48	D09
D02	Pin 32	Pin 23	D02	D10	Pin 66	Pin 49	D10
WP / -IOIS16	Pin 33	Pin 24	WP / -IOIS16 (-IOCS16)	-CD2	Pin 67	Pin 25	-CD2
GND	Pin 34	Pin 50	GND	GND	Pin 68	Pin 50	GND

Notes: A signal name appearing alone is a PC Card memory mode, PC Card I/O and True IDE signal name
A signal appearing alone before a "(" is both a PC Card memory mode and PC Card I/O mode signal name.
A signal appearing before "/" is a PC Card memory mode signal name.
A signal appearing after "/" is a PC Card I/O mode signal name.
A signal appearing in "( )" is a True IDE mode signal name.
A signal appearing in "(D)" is a True IDE mode DMA-only signal name.

7.4 CF Adapter Design Considerations

It is recommended that the 68-pin PCMCIA to 50-pin CF adapter board be constructed with a multi-layer board having a ground plane along with ground traces between signals on the top and bottom of this board for electrical cross-talk isolation.

8 Appendix

8.1 Differences between CF/CF+ and PC Card, and between CF-ATA and PC Card-ATA/True IDE

This section details differences between CF/CF+ vs. PC Card, CF-ATA vs. PC Card ATA and between CF-ATA vs. True IDE.

8.1.1 CF/CF+ Electrical Differences

8.1.1.1 TTL Compatibility

CF is not TTL compatible, it is a purely CMOS interface. Refer to Section 4.3 of this specification.

8.1.1.2 Pull-Up Resistor Input Leakage Current

The minimum pull-up resistor input leakage is 50k ohms rather than the 10k ohms stated in the PCMCIA PC Card specification.

8.1.1.3 Wait Width Time

The Wait Width Time for CompactFlash Storage Cards is 350 ns and is 3μs for CF+ Cards, rather than 12 μs as stated in the PCMCIA PC Card specification.

8.1.2 ATA Functional Differences

8.1.2.1 Additional Set Features Codes in CF-ATA

The following Set Features codes are not PC Card ATA or True IDE, but provide additional functionality in CF-ATA.

- 69h, Accepted for backward compatibility
- 96h, Accepted for backward compatibility
- 97h, Accepted for backward compatibility
- 9Ah, Set the host current source capability

8.1.2.2 Additional Commands in CF-ATA

The following commands are not standard PC Card ATA commands, but provide additional functionality in CF-ATA.

The command codes for the commands below are defined as vendor unique in PC Card ATA/True IDE.

- C0h, Erase Sectors
- 87h, Translate Sector
- F5h, Wear Level

The command codes for the commands below are defined as reserved in PC Card ATA/True IDE:

- 03h, Request Sense

- 38h, Write Without Erase
- CDh, Write Multiple Without Erase

8.1.2.3 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in PC Card ATA/True IDE.

8.1.2.4 Recovery from Sleep Mode

For CF Storage devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

8.2 Differences Between CompactFlash Storage Cards and CF+ Cards

CompactFlash and other Data Storage Cards shall have their Configuration Registers at offset 200h. On non-data storage CF+ Cards the location of the Configuration Registers is determined by parsing the CIS (Tuples).

CompactFlash and other Data Storage Cards need to support a Maximum Wait Width pulse of 350 ns, whereas non-data storage CF+ Cards only need to support a 3 µs pulse.

CompactFlash and other Data Storage Cards shall support all three access modes, memory, I/O and True IDE, whereas non-data storage CF+ Cards only need to support memory and I/O access (True IDE mode is optional).

8.3 Term Definitions

Identify Device – The name used for ATA Command Code ECh in this and future revisions of this specification. Was formerly referred to as Identify Drive.

Identify Drive – The name used for ATA Command Code ECh, the Identify Device command, in previous revisions of this specification. Also referred to as ID Drive.

mandatory – A keyword indicating items to be implemented as defined by this standard.

may – A keyword that indicates flexibility of choice with no implied preference.

obsolete – A keyword used to describe bits, bytes, fields, and code values that no longer have consistent meaning or functionality from one implementation to another. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility. An obsolete bit, byte, field, or command shall never be reclaimed for any other use in any future standard. Obsolete commands should not be used by the host. Commands defined as obsolete in previous standards may be command aborted by devices conforming to this standard. However, if a device does not command abort an obsolete command, the minimum that is required by the device in response to the command is command completion.

optional - A keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

reserved - A keyword indicating reserved bits, bytes, words, fields, and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word, or field shall be set to zero, or in

accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted.

shall - A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other standard conformant products.

should - A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

UDMA – Ultra DMA.

Ultra DMA data burst - The period in an Ultra DMA transfer from the assertion of (-)DMACK by the host during the assertion of (-)DMARQ by the card to the subsequent negation of (-)DMACK.

8.4 Bibliography

Content Protection for Recordable Media (CPRM) documents:

Content Protection for Recordable Media, Introduction and Common Cryptographic Elements Book

Content Protection for Recordable Media, Portable ATA Storage Book

Content Protection for Recordable Media, C2 Block Cipher Specification

Content Protection for Recordable Media (CPRM) documents are published by:

4C Entity, LLC

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Fax: 408-779-9291

CPRM documents may be obtained at http://www.lmicp.com.

9 Revision History

Revision Level	Changes
1.0	Initial Release.
1.1	General editorial changes; addition of connector drawings.
1.2	Correction of millimeter to inch conversions on drawings; general editorial changes.
1.3	Added CF Type II drawing and dimensions; added CF adapter bulk resistance measurement instructions; added datum A at card socket to drawings.
1.4	Added CF+ Specifications. Added updated ATA Command set. Changed name to CF+ & CompactFlash, incorporated comments regarding Power and True IDE mode. Editorial changes. Added CompactFlash vs. CF+ Appendix. Added power measurement schematic. Added note regarding CF Type II to PCMCIA adapter. Added CF Type II host connector. Updated Figure 16, “Surface Mount Right Angle CF/CF+ Type I Card Slot Header” drawing.
2.0	Added support for many ATA-4 features including updated ID Drive information, additional PIO modes, additional Set Features options and additional commands. Corrected inconsistencies and errors in signal naming, signal descriptions, host signal termination and card signal termination. Corrected inconsistencies and errors in numbering and cross-references. Added adapter for CF Type II to PCMCIA Type II. Added Key Management Feature Set commands and descriptions. Added longer and extended mechanical form-factors. Changed format of CF Adapter table. Corrected formatting, spelling and grammatical inconsistencies. Corrected inconsistencies in Figures 3, 4, 17 and 30.
2.1	Added True IDE Mode Multiword DMA. Obsolete Twin Card feature Change Driver Specification to 4 ma. Made Linguistic Clarifications. Added Alerts for ID Drive Word 0 and Set Features 09h, 89h Added Minimum Inverse Insertion Force specified as 43.2 N. Clarified Reset Pull-up Handling Added Acknowledgement of Contributors
3.0	Added Ultra DMA Diagrams and Text using CFA terminology Added Advanced Timing Modes Diagrams and Text using CFA terminology. Fixed borders and placement of diagrams Propagated Identify Device Language from 2.1 Release Changed ID Drive Word 0 to allow non 848Ah values.

	Changed captions, footnotes, cross-references to CFA standard. Expanded Signal Description Table descriptions of UDMA signals. Fixed document automation and cross reference problems. Added CRC logic description from ATA-4 specification for Ultra-DMA Removed ATA-4 cross-references from preliminary diagrams and placed referenced language from section 9 of ATA spec in paragraphs before diagrams. Adjusted tables and figures to fit in standard margins. Added section 5.2.1 on representing Extended Speed Memory Modes in CIS. Updated Section 4.7 to incorporate Ultra DMA transfers.
3.1	Changed remaining references to PCMCIA modes into PC Card mode references for consistency and clarification as PCMCIA now publishes several card standards. Cleaned up reported inconsistencies and errors.
4.0	Added PC Card UDMA modes 0 to 6 and True IDE modes 5 and 6. Cleanup of UDMA language and consistency. Applied CF Advanced Timing Mode restrictions to all UDMA modes 3 and above. Corrected inadvertent discrepancies with ATA UDMA. Corrected inadvertently exchanged UDMA timing diagrams.
4.1	Corrected IO Type description for True IDE mode IORDY during UDMA data bursts and DSTROBE pin description in IO table (Table 4). Corrected -DDMARDY, DSTROBE signal descriptions in signal description table (Table 5) Reformatted table 7 (preparation for Power mode change) Added note 6 to timing table related to IORDY release in True IDE mode. Clarified language regarding UDMA signaling and True IDE mode DSTROBE assertion requirements Corrected UDMA burst out description (IORD -> IOWR) Corrected polarity of DMARQ signal in True IDE UDMA truth table (Table 40) Added bit 2 of word 53 ID Device info according to ATA-4 spec Added bit 15 of word 164 to indicate PCMCIA UDMA supported bits valid Gave last 8 ID Device words reserved for CF back to T13 Added Power Enhanced CF Storage Card.